HD

60FPS

1/3-Inch 720p CMOS Image Sensor

Brief data sheet

Version 1.3

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Applications

- security and surveillance cameras
- automotive cameras

Features

- **Automatic controls** :

automatic exposure control(AEC), automatic gain control (AGC), automatic black level calibration (ABLC), automatic white balance (AWB),
auto flicker detection (AFD)

- **Programmable controls** :

exposure, gain, frame rate, horizontal mirror, vertical flip, scaling, windowing

- **Image adjusting functions** :

lens shading correction, color correction, gamma correction, hue and saturation, brightness, contrast, sharpness(edge enhancement), false color suppression, chroma suppression,

- Efficient denoising coupled with defective pixel correction
- Support for eclipse cancellation
- Support for flash strobe and output enable
- Support for serial interface compatible with I^2C
- Support for output formats :
  10-bit raw / denoised / ISP Bayer,
  YUV422, BT656, HREF, RGB565
- Support for image size :
  720p @ 60fps / 30fps / 15fps
  VGA @ 60fps / 30fps / 15fps
- Support for input clock : 12/16/24/48MHz
- On-chip phase locked loop (PLL, 96MHz)

Key specifications

- **Active pixel array** : 1280H X 720V
- **Optical format** : 1/3 inch
- **Pixel size** : 4.0um X 4.0um
- **Scan mode** : progressive
- **Shutter** : rolling shutter
- **Maximum image transfer rate** :
  720p and VGA (Bayer) : 60fps
  720p and VGA (YUV) : 30fps
- **Output interface** : 10-bit parallel
- **Output formats** : 10-bit raw / denoised / ISP Bayer, YUV422, BT656, HREF, RGB565
- **Sensitivity** : 1.8V/Lux.sec
- **SNR** : 44.8 dB
- **Dynamic range** : 66.5 dB
- **Dark current** : 13.7mV/sec@60℃
- **Input clock frequency** : 12/16/24/48MHz
- **On-chip phase locked loop (PLL):**96MHz
- **Power supply** :
  analog : 3.3V ± 10%
  core : 1.8V ± 5%
  I/O : 2.6~3.6V (3.3V Typical)
- **Power requirement** :
  active : 302mW
  standby : 511uW (master clock on)
  power down : 137uW (master clock off)
- **Temperature range** :
  operating : -40℃ ~ 100℃ (functional)

1. Signal Descriptions

Table 1-1 lists the signal descriptions and their corresponding pin names for the ZA10S10 image sensor. Refer to the “chip information” file for the package information.

Table 1-1 Signal Descriptions (sheet 1 of 2)

Name	I/O Type	Functions / Descriptions
AGND_ROW	Supply	Analog control block power ground.
AVDD_ROW	Supply	Analog control block power 3.3V with 0.1uF to AGND_ROW. †
RGND	Supply	Regulator power ground.
RVDD	Supply	Regulator power 3.3V with 0.1uF to RGND. †
PLLGND	Supply	PLL power ground.
PLLVDD	Supply	PLL control block power 1.8V with 0.1uF to PLLGND. †
DGND	Supply	Digital power ground.
DVDD	Supply	Digital power 1.8V with 0.1uF to DGND.
IOGND	Supply	I/O power ground.
AVDD_REF	Supply	Analog reference power 3.3V with 0.1uF to AGND_REF. †
AGND_REF	Supply	Analog reference power ground.
PVDD	Supply	Pixel power 3.3V with 0.1uF to AGND_REF. †
DVDD	Supply	Digital power 1.8V with 0.1uF to DGND.
DGND	Supply	Digital power ground.
IOVDD	Supply	I/O power 2.6V~3.3V with 0.1uF to IOGND. †
IOGND	Supply	I/O power ground.
FSTROBE	Output	Flash or LED strobe output.
PIXCLK	Output	Pixel clock. Data can be latched by external devices at the rising or falling edge of PIXCLK. The polarity and drivability can be controlled.
PIXCLK	Output	Pixel clock. Data can be latched by external devices at the rising or falling edge of PIXCLK. The polarity and drivability can be controlled.

†. The decoupled capacitors must be tied to the corresponding ground pins.

Table 1-1 Signal Descriptions (sheet 2 of 2)

Name	I/O Type	Functions / Descriptions
SYSCLK	Input	Master clock. (12/16/24/48 MHz)
RSTB	Input	Asynchronous system reset. All registers are set to their default values.
OUTEN	Input	Data output enable. When OUTEN is 'HIGH', D[9:0] are tri-state mode. But, sensor is operation or not.
SADR1	Input	Two-wire serial interface slave address bit5.
SADR0	Input	Two-wire serial interface slave address bit2.
SCLK	Input	Two-wire serial interface clock.
STDBY	Input	Power down operation. When STDBY='1' there is neither current-flow in any analog circuit branches, nor any beat of digital clock. D[9:0] and PIXCLK, HSYNC, VSYNC pins can be controlled to be all '1', '0' or tri-state. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
D0	I/O	Parallel pixel data output 0.
D1	I/O	Parallel pixel data output 1.
D2	I/O	Parallel pixel data output 2.
D3	I/O	Parallel pixel data output 3.
D4	I/O	Parallel pixel data output 4.
D5	I/O	Parallel pixel data output 5.
D6	I/O	Parallel pixel data output 6.
D7	I/O	Parallel pixel data output 7.
D8	I/O	Parallel pixel data output 8.
D9	I/O	Parallel pixel data output 9.
HSYNC	I/O	Horizontal synchronization output. Asserted when pixel data output is valid.
VSYNC	I/O	Vertical synchronization output.
SDATA	I/O	Two-wire serial interface data.
NC	NC	No connect