

PAC7366 NTSC/PAL DIGITAL IMAGE SOC

General Description

The PAC7366 is a low voltage, highly integrated CMOS active-pixel digital image sensor. It provides high-quality color images at VGA resolution and has outputs of NTSC/PAL interlaced composite analog video and parallel digital format that is embedded the new FinePixel™ sensor technology to perform the excellent image quality. It is available in CLCC-48L package.

The PAC7366 can be programmed via I2C™ serial control bus or by a attached SPI or I2C flash memory at startup. By programming the internal register set, it performs the exposure time for different luminance condition, offset correction DAC, programmable gain control, auto white balance and auto de-flicker.

Features

- **Output Format (analog composite video):**
 - NTSC_TV / NTSC_BT656
 - PAL_TV / PAL_BT656
- **Output Format (parallel digital):**
 - YUV/YCrCb 4:2:2
 - RGB565/555/444
- Bayer-RGB color filter array
- On-chip 10-bit pipelined A/D converter
- Integrated video encoder for NTSC/PAL with overlay capability and DAC
- On-chip manual analog gain control
- I2C™ Interface
- Interface to EEPROM through I2C™ bus
- Interface to low cost Flash through SPI and I2C bus
- **Power consumption: operating typ. TBD mW(full resolution @ 60fps)**
- ABC (Automatic Background Compensation)
- Black sun cancellation
- **DSP function:**
 - AEC & AGC
 - AWB
 - Gamma
 - Color matrix
 - Sharpness
 - De-noise
 - Color saturation
 - Defect compensation
 - Lens shading compensation
 - Auto de-flicker
 - Horizontal and vertical image flip
 - Zoom & windowing & sampling rate
- OSD (4 + 1 layers)
- PLL
- GPIO(configuration IO : pedestal, mirror, NTSC/PAL, SADDR, OSD on/off)

Key Specifications

- **Active Array Size:**
 - NTSC_TV output: 640x480 (1/4")
 - NTSC_BT656 output: 720x480 (1/4")
 - PAL_BT656 output: 720x576 (1/3")
 - PAL_TV output: 768x576 (1/3")
- **Optical format:**
 - 1/4" Lens for NTSC
 - 1/3" Lens for PAL
- **Maximum Frame Rate:**
 - NTSC: 60 fields per second
 - PAL: 50 fields per second
- **Pixel Size: 5.6um * 5.6um**
- **Lens Chief Ray Angle: 0°**
- **Scan Mode: Progressive**
- **Power Supply:**
 - Analog: typ. 2.8V
 - Core: typ. 1.8V
 - I/O: 1.7V~3.3V
- **input clock: typ. 27Mhz**
- **Pixel clock: 27Mhz**
- **Output interface:**
 - Analog composite video out, single-ended or differential
 - 8-bit parallel digital output
- **Sensitivity: 11500 mV/Lux-Sec**
- **S/N Ratio: 45 dB**
- **Dynamic range: 80 dB**
- **Package: CLCC-48L, 10.00mm x 10.00mm, 0.7mm pitch**

1. Pin Assignment

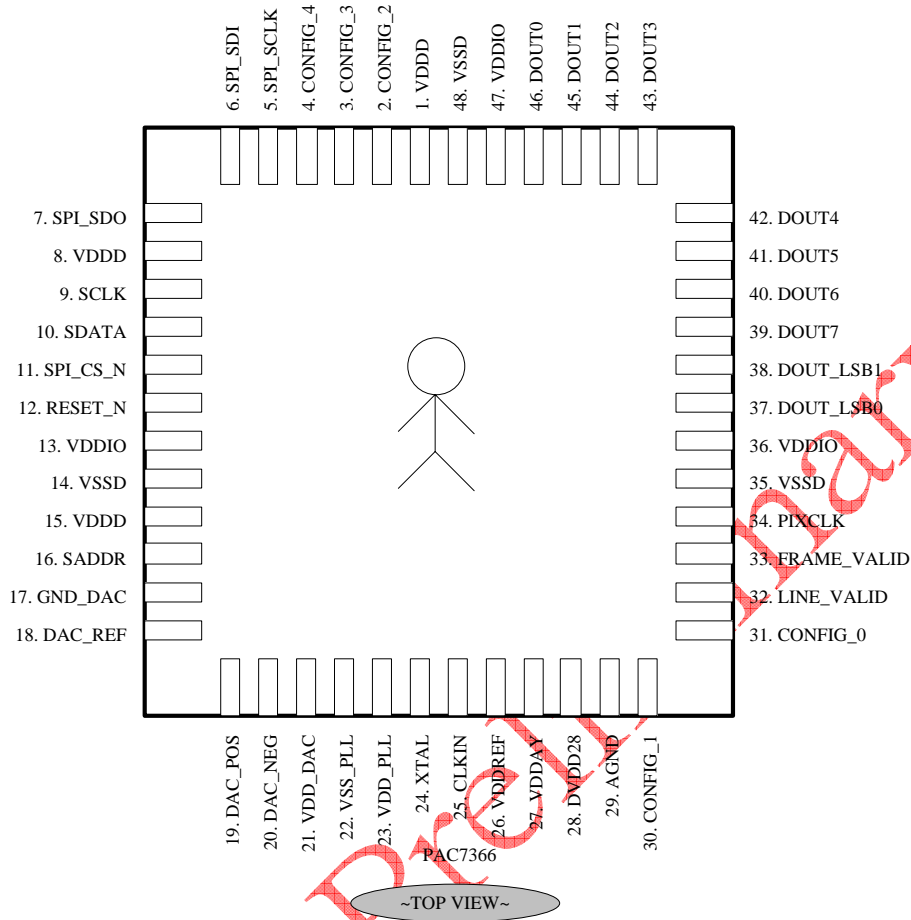


Fig.1.1 Package Pin Assignment

Pin No.	Name	Type	Description
1	VDDD	Power	Core voltage 1.8V
2	CONFIG_2	Input	Mode selection
3	CONFIG_3	Input	Mode selection
4	CONFIG_4	Input	Mode selection
5	SPL_SCLK	Output	Output clock for interfacing an external SPI memory such as FLASH/EEPROM
6	SPL_SDI	Input/PU	Data in from SPI device. Internal pull up.
7	SPL_SDO	Output	Data out to SPI device.
8	VDDD	Power	Core voltage 1.8V,
9	SCLK	Input	I2C clock
10	SDATA	Input/Output/OD	I2C data, open drain type
11	SPL_CS_N	Output	Chip select to SPI device.
12	RESET_N	Input/PU	Reset signal, active low, internal pull high.
13	VDDIO	Power	IO voltage , 2.8V
14	VSSD	GND	Digital ground
15	VDDD	Power	Core voltage 1.8V

16	SADDR	Input	I2C device ID selection: 0 : 0x90 1: 0xBA
17	GND_DAC	GND	Video DAC ground
18	DAC_REF	Output	External reference resistor for the video DAC. The DAC reference resistor should be 3.5kOhm 1% for a 75 ohm video output load
19	DAC_POS	Output	Positive video DAC output in differential mode, Video DAC output in single-ended mode.
20	DAC_NEG	Output	Negative video DAC output in differential mode, Connected a resistor to GND equal to the load resistor on DAC_POS
21	VDD_DAC	Power	Supply for Video DAC , 2.8V
22	VSS_PLL	GND	PLL ground
23	VDD_PLL	Power	Supply for PLL , 2.8V
24	XTAL	Output	If XTAL is used, XTAL is served as XTAL_OUT, otherwise it is NC
25	CLKIN	Input	Master clock input (27MHz) square or served as XTAL_IN
26	VDDREF	Power	Regulator output (2.5V) for ADC VRT/VRB/VCM driver
27	VDDAY_	Power	2.5V regulator output
28	DVDD28	Power	Analog power : 2.8V
29	AGND	GND	Analog Ground
30	CONFIG_1	Input	Mode selection
31	CONFIG_0	Input	Mode selection
32	LINE_VALID	Input/Output	Hsync
33	FRAME_VALID	Input/Output	Vsync
34	PIXCLK	Output	pixel clock output
35	VSSD	GND	Digital ground
36	VDDIO	Power	IO voltage , 2.8V
37	DOUT_LSB0	Input/Output	10bit data mode, these two extra bit make the {DOUT[7:0],DOUT_LSB1,DOUT_LSB0} as a 10 bit data for each pixel
38	DOUT_LSB1	Input/Output	
39	DOUT7	Output	pixel data output
40	DOUT6	Output	pixel data output
41	DOUT5	Output	pixel data output
42	DOUT4	Output	pixel data output
43	DOUT3	Output	pixel data output
44	DOUT2	Output	pixel data output
45	DOUT1	Output	pixel data output
46	DOUT0	Output	pixel data output
47	VDDIO	Power	IO voltage , 2.8V
48	VSSD	GND	Digital ground

2. Specifications

Absolute Maximum Ratings					
Operating Temperature		-40°C ~ 105°C			
Ambient Storage Temperature		-40°C ~ 125°C			
Supply Voltage (with respect to ground)	V _{DDA}	4.5V			
	V _{DDD}	3.0V			
	V _{DDIO}	4.5V			
All Input / Output Voltage (with respect to ground)		-0.3V to V _{DDIO} + 0.5V			
Lead-free temperature, Surface-mount process		245°C			
ESD rating, Human Body model		2000V			
DC Electrical Characteristics (Ta = 0°C ~ 70°C)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V _{DDA}	DC supply voltage – Analog	2.66	2.8	2.94	V
V _{DDD}	DC supply voltage – Digital core	1.62	1.8	1.98	V
V _{DDIO}	DC supply voltage – I/O	1.7	2.8	3.3	V
I _{DDA}	Operating Current – Analog (TBD)		TBD		mA
I _{DDD}	Operating Current – Digital (TBD)		TBD		mA
Type : IN & I/O					
V _{IH}	Input Voltage HIGH	V _{DDIO} * 0.7			V
V _{IL}	Input Voltage LOW			V _{DDIO} * 0.3	V
Type : OUT & I/O					
V _{OH}	Output Voltage HIGH	V _{DDIO} * 0.9			V
V _{OL}	Output Voltage LOW			V _{DDIO} * 0.1	V
AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f _{sysclk}	System clock frequency		27		MHz
t _{sysclk_dc}	System clock duty cycle	45		55	%
Sensor Characteristics					
Parameter		Typ.		Unit	
Sensitivity		11500		mV/Lux-Sec	
Signal to Noise Ratio		45		dB	
Dynamic Range		80		dB	

3. I2C™ Bus

PAC7366 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is “1001000” and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

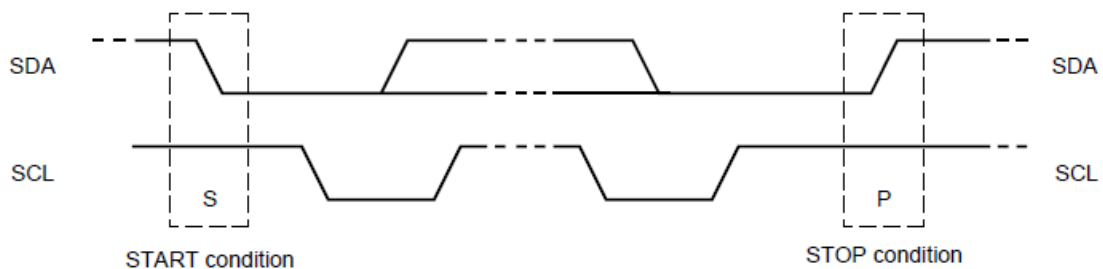


Fig.3.1 Start and Stop conditions

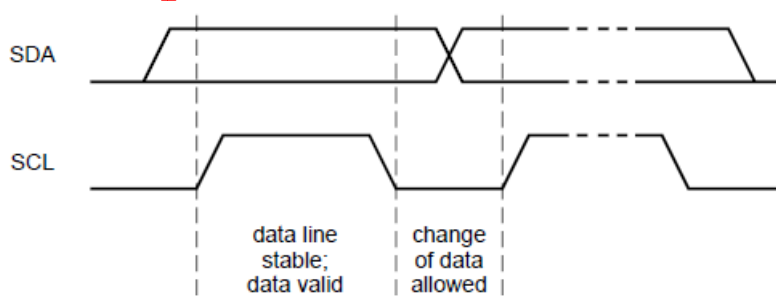


Fig.3.2 Valid Data

Data Transfer Format

Master transmits data to slave (write cycle)

- S : Start.
- A : Acknowledge by slave.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAC7366 internal control registers. (Please refer to PAC7366 register description)

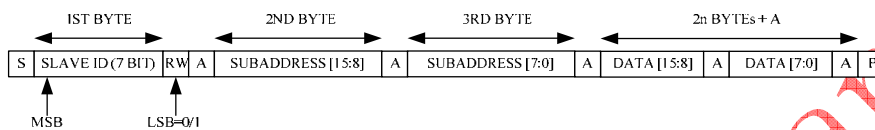


Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAC7366) issues acknowledgment, the master places 2nd and 3rd byte (Sub Address) data on SDA line. Again follow the PAC7366 acknowledgment, the master places the 16 bits data on SDA line and transmit to PAC7366 control register (address was assigned by 2nd and 3rd byte). After PAC7366 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAC7366 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAC7366 can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

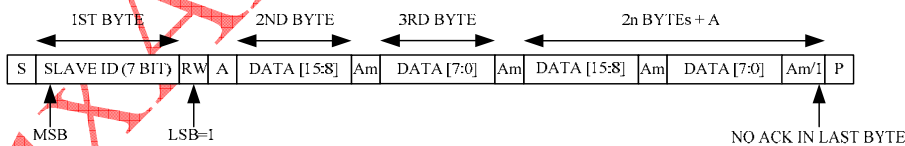


Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 16 bits DATA was also placed on SDA line by PAC7366. The 16 bits data was read from PAC7366 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAC7366 place the next 16 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAC7366) must releases SDA line to master to generate STOP condition.

I2C™ Bus Timing

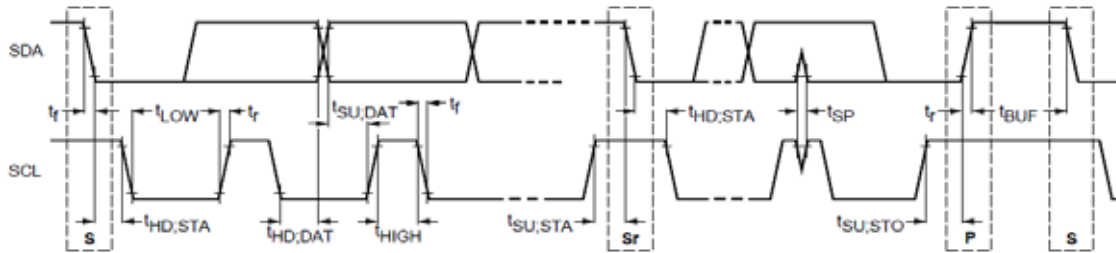


Fig.3.5 Definition of timing for F/S-mode devices on the I2C-bus.

I2C™ Bus Timing Specification				
Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	μs
Low period of the SCL clock.	t_{LOW}	4.7	-	μs
High period of the SCL clock.	t_{HIGH}	0.75	-	μs
Set-up time for a repeated START condition.	$t_{SU:STA}$	4.7	-	μs
Data hold time. For I2C-bus device.	$t_{HD:DAT}$	0	3.45	μs
Data set-up time.	$t_{SU:DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU:STO}$	4.0	-	μs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	μs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

4. Registers

Register Table

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0x00	0	[7:0]	PartID[15:8]	0x73	Part ID
0	0x01	1	[7:0]	PartID[7:0]	0x66	Part ID
0	0x02	2	[3:0]	VersionID[3:0]	0x00	VersionID
0	0x03	3	[3:0]	SubID[3:0]	0x0a	SubID
0	0x0f	15	[7:0]	R_AWB_Window_X[7:0]	0x90	AWB window width (by4)
0	0x11	17	[7:0]	R_AWB_Window_Y[7:0]	0x64	AWB window height (by4)
0	0x19	25	[7:0]	R_AWB_DGnR_LB_by2[7:0]	0x30	AWB digital gain lower bound for R
0	0x1a	26	[7:0]	R_AWB_DGnR_UB_by2[7:0]	0x49	AWB digital gain upper bound for B
0	0x1b	27	[7:0]	R_AWB_DGnB_LB_by2[7:0]	0x3a	AWB digital gain lower bound for B
0	0x1c	28	[7:0]	R_AWB_DGnB_UB_by2[7:0]	0x78	AWB digital gain upper bound for R
0	0x1f	31	[4]	R_DeNoiseEn	0x10	DeNoise Enable
0	0x20	32	[7:0]	R_DeNoise_Str_G[7:0]	0x03	Denoise Strength (for color G)
0	0x23	35	[7:0]	R_DeNoise_Str_RB[7:0]	0x04	Denoise Strength (for color R/B)
0	0x29	41	[0]	R_ISP_Gamma_EnH	0x01	ISP gamma correction enable
0	0x2a	42	[7:0]	R_ISP_Y00	0x0d	ISP Gamma Y0
0	0x2b	43	[7:0]	R_ISP_Y01	0x19	ISP Gamma Y1
0	0x2c	44	[7:0]	R_ISP_Y02	0x2f	ISP Gamma Y2
0	0x2d	45	[7:0]	R_ISP_Y03	0x53	ISP Gamma Y3
0	0x2e	46	[7:0]	R_ISP_Y04	0x62	ISP Gamma Y4
0	0x2f	47	[7:0]	R_ISP_Y05	0x6f	ISP Gamma Y5
0	0x30	48	[7:0]	R_ISP_Y06	0x7c	ISP Gamma Y6
0	0x31	49	[7:0]	R_ISP_Y07	0x87	ISP Gamma Y7
0	0x32	50	[7:0]	R_ISP_Y08	0x9a	ISP Gamma Y8
0	0x33	51	[7:0]	R_ISP_Y09	0xaa	ISP Gamma Y9
0	0x34	52	[7:0]	R_ISP_Y10	0xb8	ISP Gamma Y10
0	0x35	53	[7:0]	R_ISP_Y11	0xc5	ISP Gamma Y11
0	0x36	54	[7:0]	R_ISP_Y12	0xd8	ISP Gamma Y12
0	0x37	55	[7:0]	R_ISP_Y13	0xe8	ISP Gamma Y13
0	0x38	56	[7:0]	R_ISP_Y14	0xf5	ISP Gamma Y14
0	0x47	71	[1:0]	R_AWB_Speed	0x34	AWB adjust speed. The more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	0x49	73	[7:0]	R_AWB_SumRatio_B	0x80	AWB B sum ratio = 128/X
0	0x4a	74	[7:0]	R_AWB_SumRatio_R	0x80	AWB R sum ratio = 128/X
0	0x4d	77	[7:0]	R_AWB_CbThdL[7:0]	0x64	AWB region test Cb Low threshold -128 ~ +127 (2's complement)
0	0x4e	78	[7:0]	R_AWB_CrThdL[7:0]	0x87	AWB region test Cr Low threshold -128 ~ +127 (2's complement)
0	0x4f	79	[7:0]	R_AWB_CbCrThdL[7:0]	0x00	AWB region test Cb+Cr Low threshold -128 ~ +127 (2's complement)
0	0x50	80	[7:0]	R_AWB_CbThdH[7:0]	0x75	AWB region test Cb High threshold -128 ~ +127 (2's complement)
0	0x51	81	[7:0]	R_AWB_CrThdH[7:0]	0x96	AWB region test Cr High threshold -128 ~ +127 (2's complement)
0	0x52	82	[7:0]	R_AWB_CbCrThdH[7:0]	0xff	AWB region test Cb+Cr High threshold -128 ~ +127 (2's complement)
0	0x53	83	[7:0]	R_Ylow	0x1e	Low bound of "light-pixel"Y in AWB
0	0x54	84	[7:0]	R_Yhigh	0xff	High bound of "light-pixel"Y in AWB
0	0x63	99	[5]	R_ISP_EnH	0x20	ISP enable
0	0x66	102	[4]	R_AE_EnH	0x00	AE enable
0	0x6d	109	[7:0]	R_AG_stage_UB	0x3f	AG_stage upper bound at max AE_stage
0	0x6f	111	[7:0]	R_Ytar8bit	0x82	0~255, Target luminance of AE
0	0x72	114	[0]	R_AWB_EnH	0x00	Auto-white balance enable
0	0x79	121	[7:0]	R_ISP_HOffset[7:0]	0x19	ISP Hsize Offset
0	0x7b	123	[7:0]	R_ISP_VOffset[7:0]	0x04	ISP Vsize Offset
0	0x81	129	[5:4]	R_AE_Speed	0x00	AE speed, the more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	0x8f	143	[7:0]	R_ImgEffect_c0	0x00	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
0	0x90	144	[7:0]	R_ImgEffect_c1	0x00	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
0	0x91	145	[7:0]	R_ImgEffect_c2	0x00	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
0	0x93	147	[3:0]	R_ImgEffectMode	0x00	Image Effect mode 0: monochrome 1: negative 2: x-ray

						3: Sepia/Cold/Warm/Sunset 6: Solarize 10: Pixelate (ISP_UpdateFlag=1, update)
0	0x94	148	[0]	R_ISP_ImgEffect_En	0x00	(ISP_UpdateFlag=1, update)
0	0x97	151	[4]	R_Shading_EnH	0x01	Lens shading enable
0	0x98	152	[4]	R_VFLIP	0x00	Vertical flip
0	0x98	152	[5]	R_HFLIP	0x00	Horizontal flip
0	0x99	153	[6:0]	R_OffsetX_R[6:0]	0x00	Horizontal distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	0x9a	154	[6:0]	R_OffsetY_R[6:0]	0x00	Vertical distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	0x9b	155	[6:0]	R_OffsetX_G[6:0]	0x00	Horizontal distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	0x9c	156	[6:0]	R_OffsetY_G[6:0]	0x00	Vertical distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	0x9d	157	[6:0]	R_OffsetX_B[6:0]	0x00	Horizontal distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	0x9e	158	[6:0]	R_OffsetY_B[6:0]	0x00	Vertical distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	0x9f	159	[5:0]	R_LSC_R1[5:0]	0x00	Quartic parameter of R-channel
0	0xa0	160	[5:0]	R_LSC_G1[5:0]	0x00	Quartic parameter of G-channel
0	0xa1	161	[5:0]	R_LSC_B1[5:0]	0x00	Quartic parameter of B-channel
0	0xa2	162	[5:0]	R_LSC_R2[5:0]	0x50	Square parameter of R-channel
0	0xa3	163	[5:0]	R_LSC_G2[5:0]	0x50	Square parameter of G-channel
0	0xa4	164	[5:0]	R_LSC_B2[5:0]	0x50	Square parameter of B-channel
0	0xa5	165	[2:0]	R_LSFT_1[2:0]	0x04	
0	0xa6	166	[1:0]	R_LSFT_2[1:0]	0x00	
0	0xa7	167	[1:0]	R_LSFT_3[1:0]	0x01	
0	0xa8	168	[1:0]	R_LSFT_4[1:0]	0x01	
0	0xcx	204	[7:0]	DGn_R_vs[7:0]	0x00	R Digital Gain sync by vsync
0	0xcd	205	[0]	DGn_R_vs[8]	0x00	R Digital Gain sync by vsync
0	0xce	206	[7:0]	DGn_G_vs[7:0]	0x00	G Digital Gain sync by vsync
0	0xcf	207	[0]	DGn_G_vs[8]	0x00	G Digital Gain sync by vsync
0	0xd0	208	[7:0]	DGn_B_vs[7:0]	0x00	B Digital Gain sync by vsync
0	0xd1	209	[0]	DGn_B_vs[8]	0x00	B Digital Gain sync by vsync
0	0xe0	224	[7:0]	R_ISP_HSize[7:0]	0x80	ISP output Horizontal size(before skip function)
0	0xe1	225	[1:0]	R_ISP_HSize[9:8]	0x02	ISP output Horizontal size(before skip function)
0	0xe2	226	[7:0]	R_ISP_VSize[7:0]	0xe0	ISP output Vertical size(before skip function)
0	0xe3	227	[1:0]	R_ISP_Vsize[9:8]	0x01	ISP output Vertical size(before skip function)
0	0xef	239	[2:0]	R_RegBankSel	0x00	Register Bank Select 0: ISP1 Register Bank (default) 1: Sensor Register Bank 2: ISP2 Register Bank
1	0x08	8	[4:0]	Cmd_Global	0x00	Global gain control signal
1	0x09	9	[1:0]	Cmd_fgh	0x0	Front gain control signal ; fgh=0/2/3
1	0x0A	10	[1:0]	Cmd_ggh	0x0	Coase tuning global gain control signal ; ggh=0/2/3
1	0x22	34	[0]	Cmd_HFlip	0x0	Horizontal Flip
1	0x25	37	[0]	Cmd_VFlip	0x0	Vertical Flip
2	0x08	8	[7:0]	R_ImgEffect_Y_offset	0x00	
2	0x09	9	[7:0]	R_ImgEffect_U_offset	0x00	
2	0x0a	10	[7:0]	R_ImgEffect_V_offset	0x00	
2	0x0b	11	[0]	R_ISP_ImgEffect_1_En	0x00	
2	0x2a	42	[7]	R_ISP_Edge_En0	0x01	ISP edge enhancement enable
2	0x2f	47	[4:0]	R_AE_stage_LL[4:0]	0x13	(AE_stage >= R_AE_stage_LL) && (AG_stage >= R_AG_stage_LL) =>Low Light
2	0x30	48	[4:0]	R_AE_stage_NL[4:0]	0x11	(AE_stage <= R_AE_stage_NL) && (AG_stage <= R_AG_stage_NL) =>Normal Light
2	0x32	50	[7:0]	R_AG_stage_LL[7:0]	0x10	(AE_stage >= R_AE_stage_LL) && (AG_stage >= R_AG_stage_LL) =>Low Light
2	0x33	51	[7:0]	R_AG_stage_NL[7:0]	0x00	(AE_stage <= R_AE_stage_NL) && (AG_stage <= R_AG_stage_NL) =>Normal Light
2	0x56	86	[4:0]	R_EdgeRatio_Delta[4:0]	0x08	Increment when AE/AG state change
2	0x57	87	[4:0]	R_EdgeRatio_LL[4:0]	0x04	Edge ratio @Low Light
2	0x58	88	[4:0]	R_EdgeRatio_NL[4:0]	0x0a	Edge ratio @Normal Light
2	0x5a	90	[4:0]	R_Edge_th_Delta[4:0]	0x08	Increment when AE/AG state change
2	0x5b	91	[7:0]	R_Edge_th_LL[7:0]	0x0a	Edge threshold @ Low Light
2	0x5c	92	[7:0]	R_Edge_th_NL[7:0]	0x08	Edge threshold @ Normal Light
2	0x5e	94	[4:0]	R_Saturation_Delta[4:0]	0x01	Increment when AE/AG state change

2	0x5f	95	[4:0]	R_Saturation_LL[4:0]	0x0b	Color Saturation @ Low Light
2	0x60	96	[4:0]	R_Saturation_NL[4:0]	0x16	Color Saturation @ Normal Light
2	0x62	98	[4:0]	R_Shading_CP_R_Delta[4:0]	0x02	Increment when AE/AG state change
2	0x63	99	[3:0]	R_Shading_CP_R_NL[3:0]	0x0f	Shading compensation percentage @Normal Light
2			[7:4]	R_Shading_CP_R_LL[3:0]	0x00	Shading compensation percentage @Low Light
2	0x64	100	[0]	R_Contrast_En	0x01	Contrast Enable
2	0x69	105	[7:0]	R_Brightness_LL[7:0]	0x00	Brightness @ Low Light
2	0x6a	106	[7:0]	R_Brightness_NL[7:0]	0x00	Brightness @ Normal Light
2	0x9b	155	[1:0]	R_ISP_WOI_HSize[9:8]	0x02	(ISP2_UpdateFlag=1, update)
2	0x9c	156	[7:0]	R_ISP_WOI_HSize[7:0]	0x80	(ISP2_UpdateFlag=1, update)
2	0x9d	157	[1:0]	R_ISP_WOI_VSize[9:8]	0x01	(ISP2_UpdateFlag=1, update)
2	0x9e	158	[7:0]	R_ISP_WOI_VSize[7:0]	0xe0	(ISP2_UpdateFlag=1, update)
2	0x9f	159	[1:0]	R_ISP_WOI_HOffset[9:8]	0x00	(ISP2_UpdateFlag=1, update)
2	0xa0	160	[7:0]	R_ISP_WOI_HOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
2	0xa1	161	[1:0]	R_ISP_WOI_VOffset[9:8]	0x00	(ISP2_UpdateFlag=1, update)
2	0xa2	162	[7:0]	R_ISP_WOI_VOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
2	0xbf	191	[1]	R_UV_Swap	0x00	U V Swap
2			[2]	R_YC_Swap	0x01	Y C Swap
2	0xc0	192	[3:0]	R_RGB565_mode[3:0]	0x00	RGB565_mode
2	0xc0	192	[5:4]	R_Format_Sel	0x00	Output Data format select 0:YUV 1:RGB565 2:RGB555 3:RGB444 (ISP2_UpdateFlag=1, update)
2	0xc1	193	[0]	R_Vsync_INV	0x01	Vsync inverse
2	0xc1	193	[1]	R_Hsync_INV	0x01	Hsync inverse
2	0xc1	193	[2]	R_Pxclk_INV	0x00	Pxclk inverse
3	0x02	2	[0]	R_CCMA_Sign[8]	0x00	ACCM Base matrix coefficient
3	0x03	3	[7:0]	R_CCMA_Sign[7:0]	0x33	ACCM Base matrix coefficient
3	0x04	4	[7:0]	R_CCMA0_0[7:0]	0x2c	ACCM Base matrix coefficient
3	0x05	5	[7:0]	R_CCMA0_1[7:0]	0x2c	ACCM Base matrix coefficient
3	0x06	6	[7:0]	R_CCMA0_2[7:0]	0x28	ACCM Base matrix coefficient
3	0x07	7	[7:0]	R_CCMA1_0[7:0]	0x0b	ACCM Base matrix coefficient
3	0x08	8	[7:0]	R_CCMA1_1[7:0]	0x39	ACCM Base matrix coefficient
3	0x09	9	[7:0]	R_CCMA1_2[7:0]	0x44	ACCM Base matrix coefficient
3	0x0a	10	[7:0]	R_CCMA2_0[7:0]	0x40	ACCM Base matrix coefficient
3	0x0b	11	[7:0]	R_CCMA2_1[7:0]	0x34	ACCM Base matrix coefficient
3	0x0c	12	[7:0]	R_CCMA2_2[7:0]	0x0c	ACCM Base matrix coefficient
5	0x00	0	[0]	r_TXF_En	0x0	0: Disable lens distortion, ccir656 output from ISP 1: Enable lens distortion, ccir656 output from TXF
6	0x00	0	[2:0]	reg_tv_mode	0x0	NTSC_M=0; (v, pedestal on) NTSC_J=1; (v, pedestal off) PAL_M=2; PAL_N=4; (v, pedestal on) PAL_NC=5; PAL_BDGHI=6; (v, pedestal off)
6	0x01	1	[0]	reg_tv_e	0x0	1: TV Encoder Enable
7	0x00	0	[0]	r_og_enable	0x1	overlay generator enable signal
7	0x12	18	[0]	r_layer_show_1	0x1	show enable signal of layer 1
7			[1]	r_layer_show_2	0x1	show enable signal of layer 2
7			[2]	r_layer_show_3	0x1	show enable signal of layer 3
7			[3]	r_layer_show_4	0x1	show enable signal of layer 4
7			[4]	r_layer_show_5	0x1	show enable signal of layer 5 (number layer)
7	0x97	151	[7:0]	r_Y_num_char[7:0]	0x00	Y value of word color in number layer
7	0x98	152	[7:0]	r_Cb_num_char[7:0]	0x00	Cb value of word color in number layer
7	0x99	153	[7:0]	r_Cr_num_char[7:0]	0x00	Cr value of word color in number layer
7	0x9a	154	[7:0]	r_Y_num_back[7:0]	0x00	Y value of background color in number layer
7	0x9b	155	[7:0]	r_Cb_num_back[7:0]	0x00	Cb value of background color in number layer
7	0x9c	156	[7:0]	r_Cr_num_back[7:0]	0x00	Cr value of background color in number layer
7	0xc1	193	[7:0]	r_number_char_2_1[7:0]	0x00	1st and 2nd number character
7	0xc2	194	[7:0]	r_number_char_4_3[7:0]	0x00	3rd and 4th number character
7	0xc3	195	[7:0]	r_number_char_6_5[7:0]	0x00	5th and 6th number character
7	0xc4	196	[7:0]	r_number_char_8_7[7:0]	0x00	7th and 8th number character
7	0xc5	197	[7:0]	r_number_char_10_9[7:0]	0x00	9th and 10th number character
7	0xc6	198	[7:0]	r_number_char_12_11[7:0]	0x00	11th and 12th number character
7	0xc7	199	[7:0]	r_number_char_14_13[7:0]	0x00	13th and 14th number character
7	0xc8	200	[7:0]	r_number_char_16_15[7:0]	0x00	15th and 16th number character
7	0xc9	201	[7:0]	r_number_char_18_17[7:0]	0x00	17th and 18th number character

7	0xca	202	[7:0]	r_number_char_20_19[7:0]	0x00	19th and 20th number character
7	0xcb	203	[7:0]	r_number_char_22_21[7:0]	0x00	21th and 22th number character
7	0xcc	204	[4:0]	r_number_amount[4:0]	0x00	number amount in number layer
7	0xcd	205	[1:0]	r_transparency_h_num[1:0]	0x00	head bits of transparencies in number layer
7	0xce	206	[7:0]	r_transparency_num_word[7:0]	0x00	transparency of word in number layer
7	0xcf	207	[7:0]	r_transparency_num_back[7:0]	0x00	transparency of background in number layer
7	0xd0	208	[7:0]	r_target_image_num_1[7:0]	0x00	index for layer 1 overlay image access
7	0xd1	209	[7:0]	r_target_image_num_1[15:8]	0x00	index for layer 1 overlay image access
7	0xd2	210	[7:0]	r_target_image_num_2[7:0]	0x00	index for layer 1 overlay image access
7	0xd3	211	[7:0]	r_target_image_num_2[15:8]	0x00	index for layer 1 overlay image access
7	0xd4	212	[7:0]	r_target_image_num_3[7:0]	0x00	index for layer 1 overlay image access
7	0xd5	213	[7:0]	r_target_image_num_3[15:8]	0x00	index for layer 1 overlay image access
7	0xd6	214	[7:0]	r_target_image_num_4[7:0]	0x00	index for layer 1 overlay image access
7	0xd7	215	[7:0]	r_target_image_num_4[15:8]	0x00	index for layer 1 overlay image access
7	0xe0	224	[7:0]	r_flicker_period_1[7:0]	0x00	flicker time period of layer 1
7	0xe1	225	[7:0]	r_flicker_period_2[7:0]	0x00	flicker time period of layer 2
7	0xe2	226	[7:0]	r_flicker_period_3[7:0]	0x00	flicker time period of layer 3
7	0xe3	227	[7:0]	r_flicker_period_4[7:0]	0x00	flicker time period of layer 4
7	0xe4	228	[7:0]	r_flicker_period_5[7:0]	0x00	flicker time period of layer 5

5. Reference Circuit Schematic

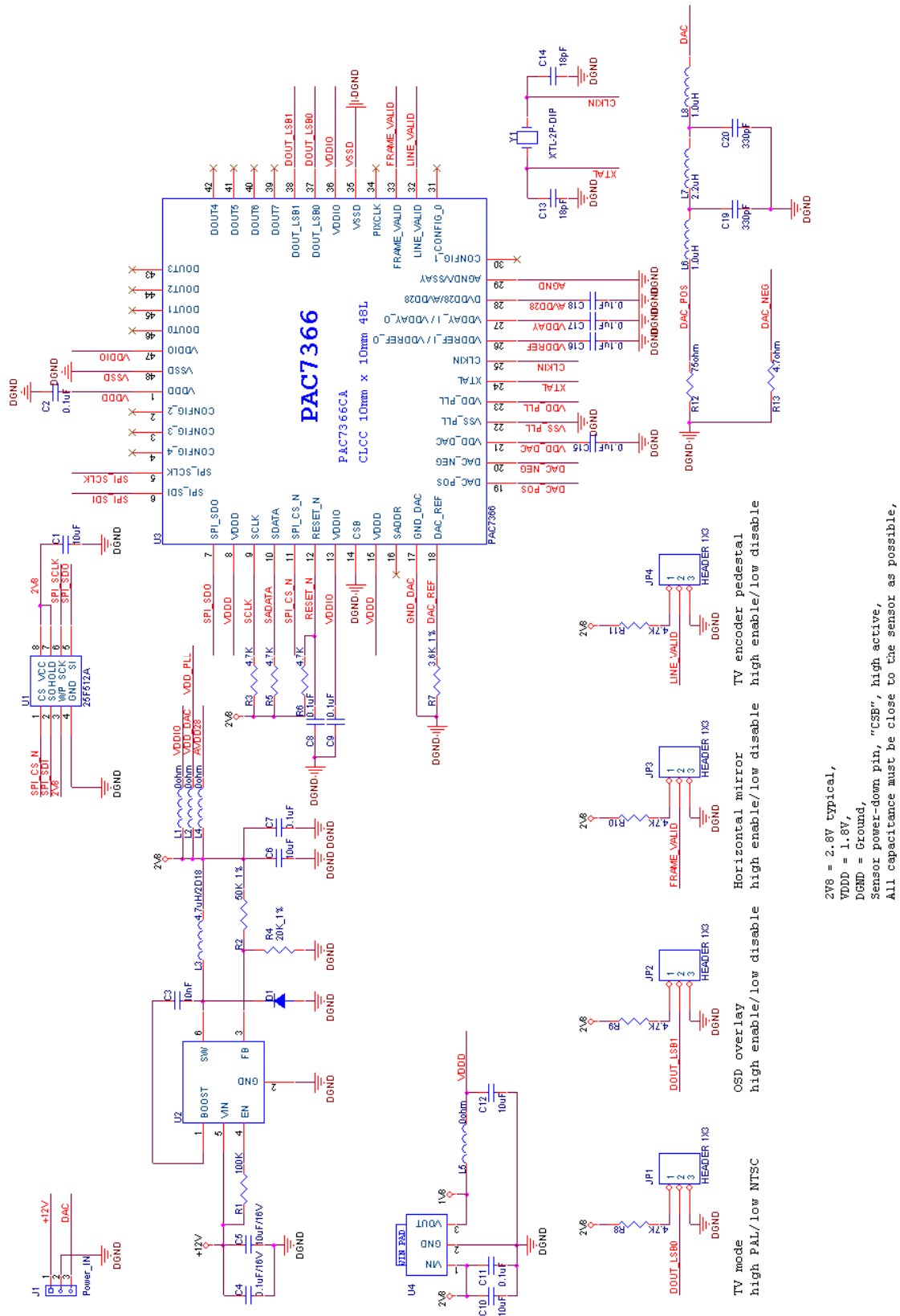


Fig.5.1 Reference Schematic

6. Internal Block Diagram

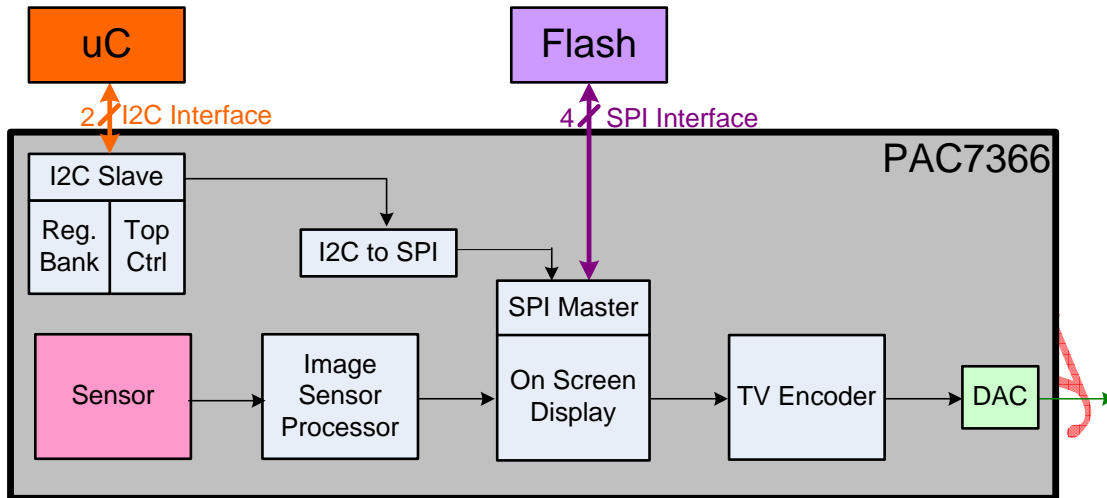


Fig.6.1 Block Diagram

7. Digital Function

- Mirror and Flip

PAC7366 provides mirror and flip modes. Mirror mode reverses the sensor data read-out order horizontally, and flip mode provides reverses it vertically.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
1	0x22	34	[0]	Cmd_HFlip	0x0	Horizontal Flip, 0 : mirror off 1 : mirror on
1	0x25	37	[0]	Cmd_VFlip	0x0	Vertical Flip, 0 : flip off 1 : flip on

Original Image	Mirrored Image	Flipped Image	Mirrored and Flipped Image
P	q	b	d

Fig.7.1 Mirror and Flip Samples

- Test Patterns generated from Image Sensor Processor, by programming a register

PAC7366 provides fixed test patterns generated by image sensor processor for test purposes. Test patterns are accessible by programming a register.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0x0C	12	[4:0]	R_ISP_TestMod	0x00	ISP test mode data generation Bit[4] : defect test pixel insertion Bit[3:0] : 0:no test; 1:white; 2:black; 3:red; 4:green; 5:blue; 6:vertical&horizontal color bar 7:random data 8:vertical gray bar 9:horizontal gray bar 12-15: motion test

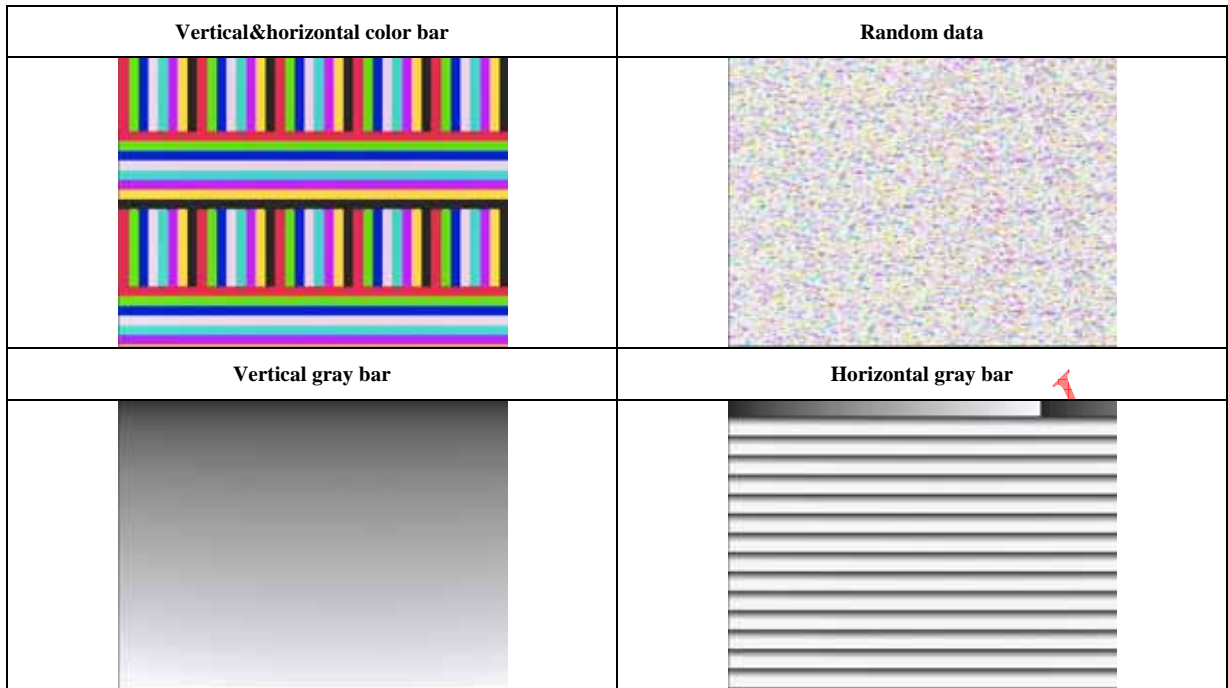


Fig.7.2 Test Patterns from Image Sensor

- **Test Patterns generated from TV encoder, by programming a register**

PAC7366 provides color bar test pattern generated by TV encoder for TV signal test purposes. Test patterns are accessible by programming a register. Color bars of NTSC and PAL are built-in to support hue and color saturation characterization and each consists of seven color bars (white, yellow, cyan, green, magenta, red, and blue)

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
6	0x11	17	[2]	reg_ccir656_src	0	0: CCIR656_SRC_Sensor 1: CCIR656_SRC_ColorBar

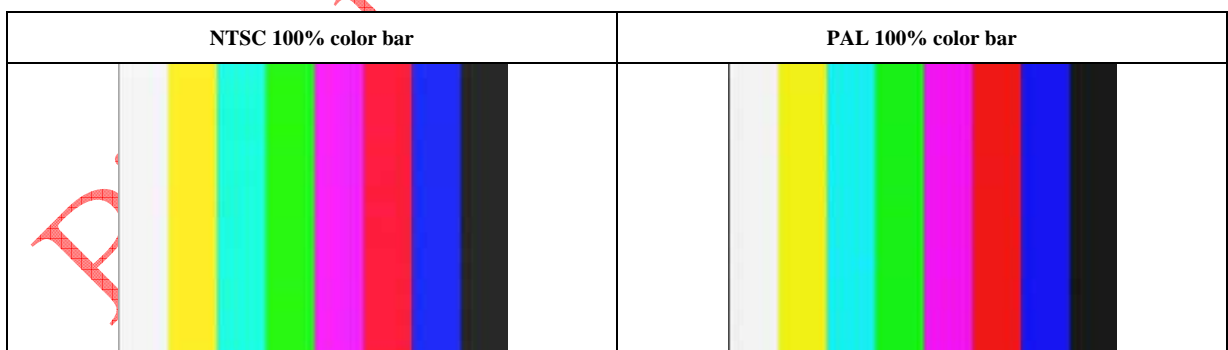


Fig.7.3 Test Patterns from TV Encoder

8. Sensor Pixel Array Structure

The active pixel array is 640 x 480 pixels for NTSC_TV, 768 x 576 pixels for PAL_TV. The active border is for color interpolation, defect, denoise and edge enhancement.

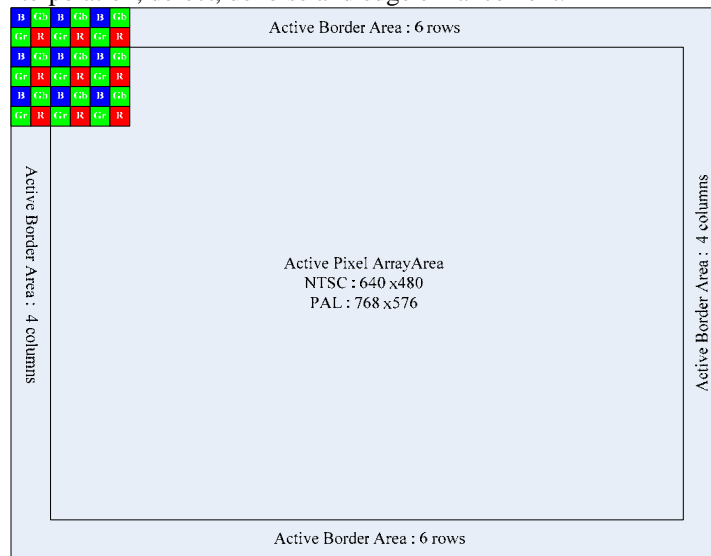


Fig.8.1 Sensor Pixel Array

9. Auto Exposure Control and Auto Gain Control

● Auto Exposure Control

Exposure time is manually set by registers when auto exposure control is off, instead it is controlled by auto exposure time algorithm when auto exposure control is on.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0x66	102	[4]	R_AE_EnH	1	0: Auto Exposure Control off 1: Auto Exposure Control on

● Auto Gain Stage Upper Bound

Maximum gain is limited to upper bound.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0x6D	109	[7:0]	R_AG_stage_UB	0x96	48 : x16 64 : x32 80 : x64 96 : x128

Note : When AE is on.

● Global gain control, Front gain control, Coase tuning global gain control

Analog gain x1~x32.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
1	0x08	08	[4:0]	Cmd_Global	0x00	1 + (Cmd_Global[4:0]/16)
1	0x09	09	[1:0]	Cmd_fgh	0x00	0 : x1 2 : x2 3 : x4
1	0x0A	10	[1:0]	Cmd_ggh	0x00	0 : x1 2 : x2 3 : x4

Note : When AE is off

10. Digital Gain

Digital gain x1, x2, x8.

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0xdf	223	[1:0]	R_DG_manual_gain	0x00	0 : x1 1 : x2 2 : x8

11. NTSC / PAL Signal Parameters

● NTSC : H_Timing

Test Item	Description	Pattern	Unit	L-Limit	H-Limit	Nominal	Measurement
H_Timing	Sync Rise Time	75% Color Bars	n sec	100.00	300.00	200.00	133.0
	Sync Fall Time		n sec	100.00	300.00	200.00	131.0
	Sync Width		u sec	4.50	4.90	4.70	4.7
	Sync Level		IRE	37.90	42.00	39.95	40.9
	Burst Level		IRE	35.00	43.40	39.20	38.0
	Sync to Burst Start		u sec	5.20	5.40	5.30	5.4
	Burst Width		cycles	8.50	9.50	9.00	9.0
	Front Porch		u sec	0.50	2.50	1.50	1.5
Line Frequency	Sync to SetUp	u sec	8.00	11.00	9.50	9.2	
	Line Frequency	kHz	15.734	15.734	15.734	15.734	
	Field Frequency	Hz	59.94	59.94	59.94	59.94	

● PAL : H_Timing

Test Item	Description	Pattern	Unit	L-Limit	H-Limit	Nominal	Measurement
H_Timing	Sync Rise Time	75% Color Bars	n sec	100.00	300.00	200.00	139.00
	Sync Fall Time		n sec	100.00	300.00	200.00	138.00
	Sync Width		u sec	4.50	4.90	4.70	4.64
	Sync Level		mV	288.00	315.00	301.50	303.40
	Burst Level		mV	250.00	310.00	280.00	278.20
	Sync to Burst Start		u sec	5.50	5.70	5.60	5.59
	Burst Width		u sec	2.00	2.50	2.25	2.32
Line Frequency	Line Frequency	kHz	15.625	15.625	15.625	15.625	
	Field Frequency	Hz	50.00	50.00	50.00	50.00	

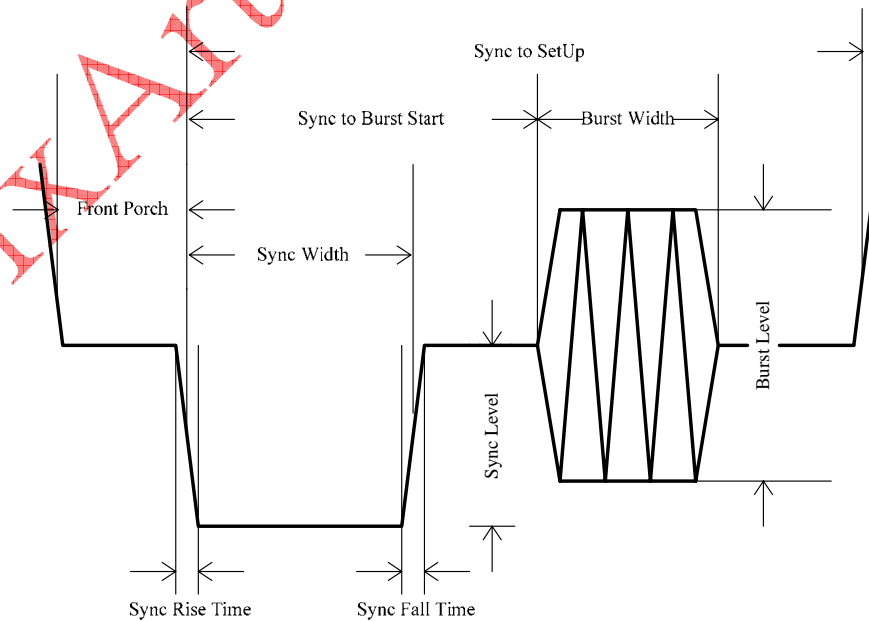


Fig.11.1 H-Timing

● NTSC : Composite Color Bar

Test Item	Description	Pattern	Unit	L-Limit	H-Limit	Nominal	Measurement
Composite Color Bar_1	Luma Level	Gray	IRE	69.2	84.6	76.9	77.9
		Yellow	IRE	62.1	75.9	69.0	70.2
		Cyan	IRE	50.5	61.7	56.1	56.9
		Green	IRE	43.4	53.0	48.2	48.8
		Magenta	IRE	32.6	39.8	36.2	36.8
		Red	IRE	25.4	31.0	28.2	28.6
		Blue	IRE	13.9	16.9	15.4	15.8
		Black	IRE	6.8	8.3	7.5	7.6
	Chroma Level	Gray	IRE	0.0	1.4	0.0	0.1
		Yellow	IRE	55.9	68.3	62.1	58.4
		Cyan	IRE	78.9	96.5	87.7	82.7
		Green	IRE	73.7	90.1	81.9	77.1
		Magenta	IRE	73.7	90.1	81.9	77.1
		Red	IRE	78.9	96.5	87.7	82.8
		Blue	IRE	55.9	68.3	62.1	58.6
		Black	IRE	0.0	1.4	0.0	0.1
	Chroma Phase	Yellow	Deg	162.1	172.1	167.1	165.0
		Cyan	Deg	278.5	288.5	283.5	282.0
		Green	Deg	235.7	245.7	240.7	240.1
		Magenta	Deg	55.7	65.7	60.7	59.2
		Red	Deg	98.5	108.5	103.5	103.1
Blue		Deg	342.1	352.1	347.1	346.0	

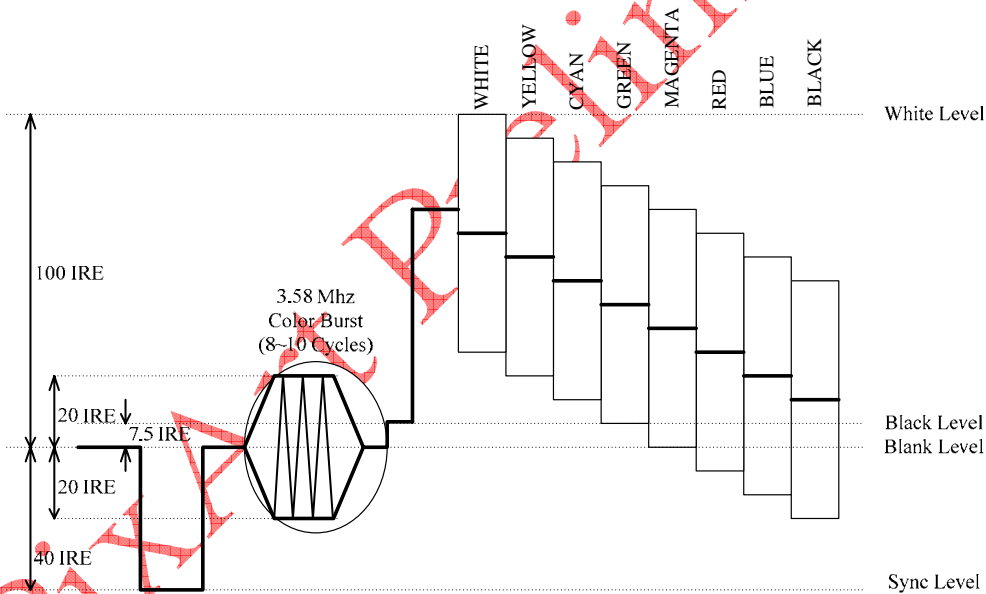


Fig.11.2 NTSC mode Color Bar

● PAL : Composite Color Bar

Test Item	Description	Pattern	Unit	L-Limit	H-Limit	Nominal	Measurement
Composite Color Bar_1	Luma Level	Gray	mV	472.5	577.5	525.0	529.8
		Yellow	mV	419	512	465.5	470.5
		Cyan	mV	331	405	368.0	370.1
		Green	mV	277	339	308.0	308.2
		Magenta	mV	195	234	217.0	219.2
		Red	mV	141	173	157.0	158.3
		Blue	mV	54	66	60.0	61.4
		Black	mV	-10	10	0.0	-0.9
	Chroma Level	Gray	mV	0.0	10.0	0.0	0.5
		Yellow	mV	423	517	470.0	437.1
		Cyan	mV	598	730	664.0	618.8
		Green	mV	558	682	620.0	577.2
		Magenta	mV	558	682	620.0	577.4
		Red	mV	598	730	664.0	619.8
		Blue	mV	423	517	470.0	438.9
		Black	mV	0.0	10.0	0.0	0.4
	Chroma Phase	Yellow	Deg	162	172	167.0	167.0
		Cyan	Deg	278	288	283.0	283.4
		Green	Deg	235	245	240.0	240.4
		Magenta	Deg	55	65	60.0	60.6
		Red	Deg	98	108	103.0	103.4
Blue		Deg	342	352	347.0	347.7	

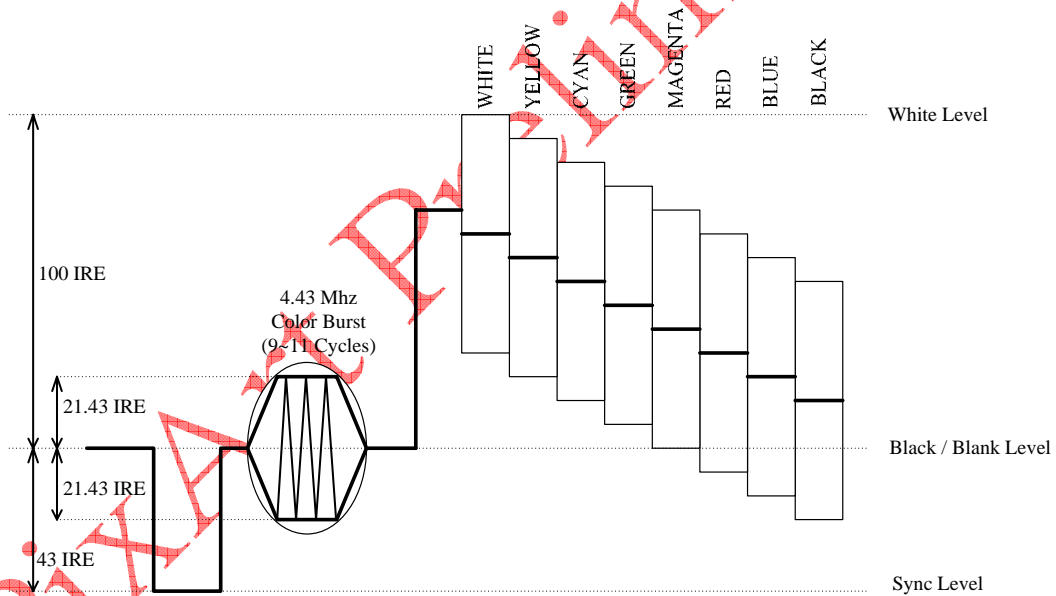


Fig.11.3 PAL mode Color Bar

12. Flash and On-Screen-Display

● Flash Devices

Registers can be loaded by Serial Flash or I2C interface.

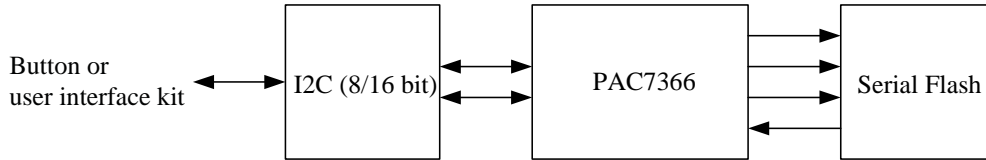


Fig.12.1 I2C and Flash Block Diagram

Table below lists Flash devices, which can support both read and write functions.

Flash Type	Density	Mfg	Device	Speed	standard	Temp. Range ()	Supply Voltage (V)
SPI	1 Mbit	NUMONYX	M25P10-A	50 Mhz	JEDEC / RES	-40~85	2.3~3.6
SPI	8 Mbit	ATMEL	AT26DF081A	70 Mhz	JEDEC / Device ID	-40~85	2.7~3.6

● On-Screen-Display

Up to four overlays may be mixed on each layer simultaneously, and a fifth layer can exist for a number character overlay. The host can modify image's size, position, color, transparency and flicker time by programming register setting.

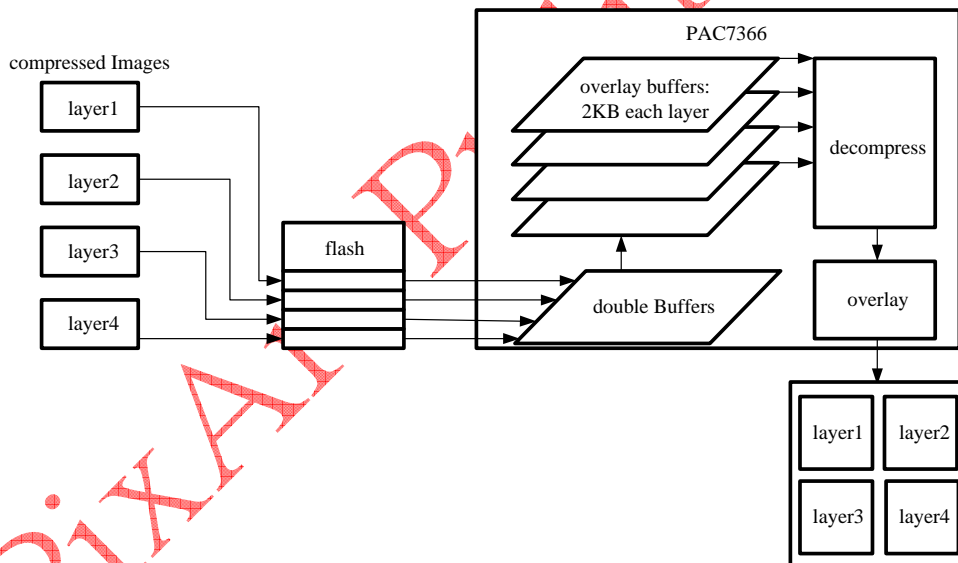


Fig.12.2 Overlay Channels

13. Package Information

● Package Mechanical Diagram

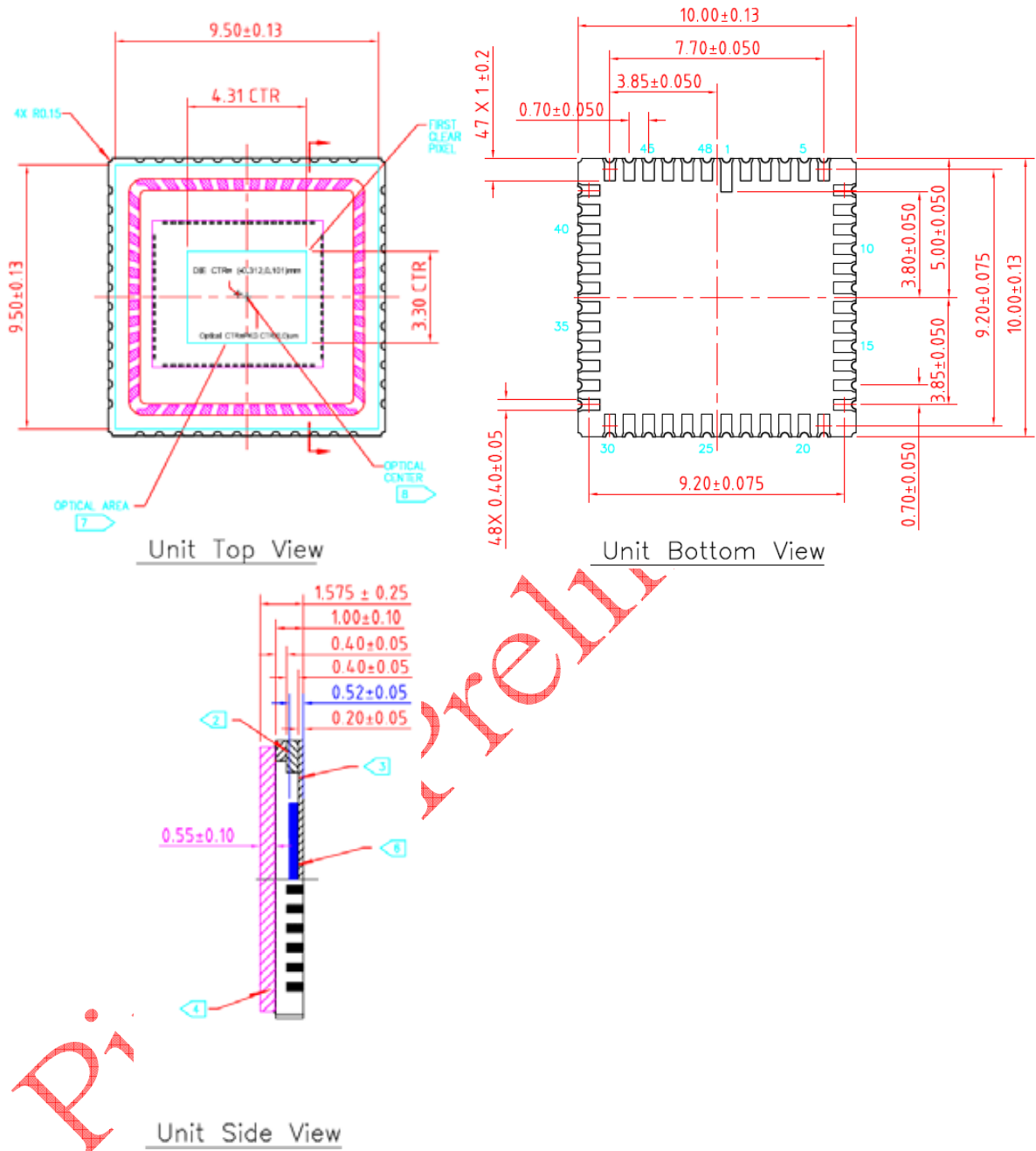


Fig.13.1 Package Mechanical Diagram

Note:

1. Dimensions in mm. dimensions in () are for reference only. Do not measure printed drawing.
2. Wall material: alumina ceramic.
3. Substrate material: alumina ceramic 0.2 thickness.
4. Lid material: borosilica glass 0.55 thickness
5. Lead finish: gold plating 0.5 microns minimum thickness.
6. Image sensor die 0.3 thickness.
7. Maximum rotation of optical area relative to package edged: 1°
Maximum tilt of optical are relative to seating plane A: 50 microns
Maximum tilt of optical are relative to top of cover glass:75 microns
8. Optical center = package center

● Recommended PCB Layout

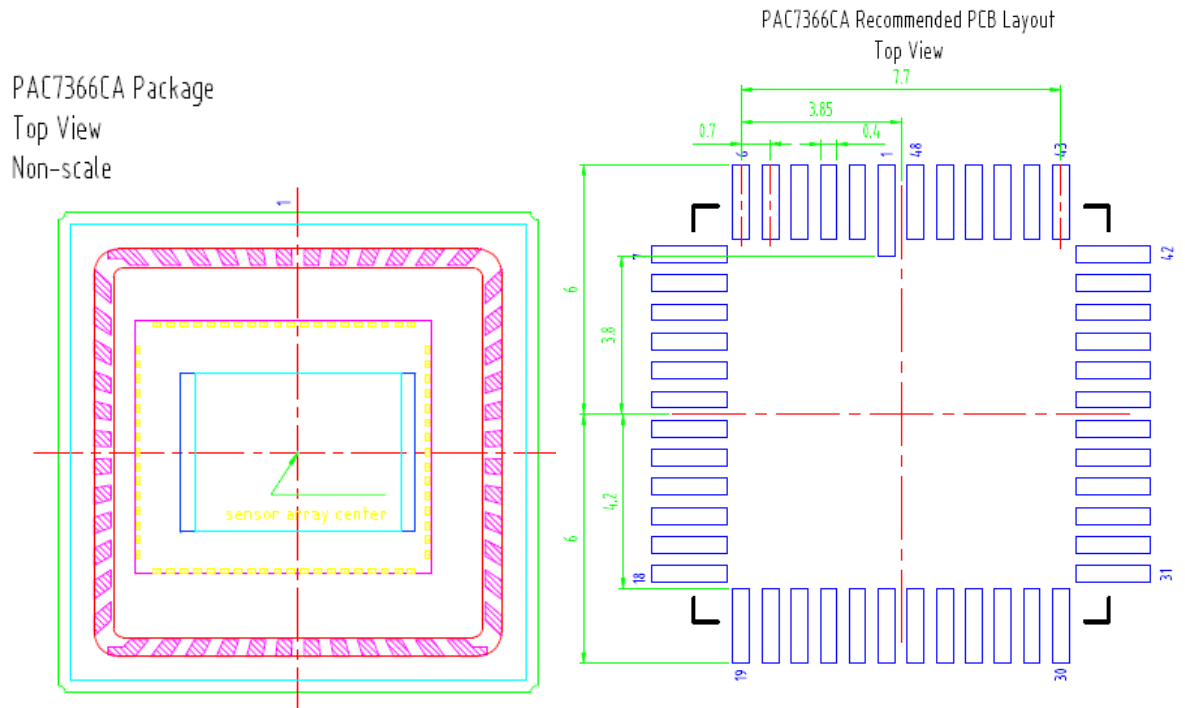


Fig.13.2 Recommended PCB Layout

Note:

- 1. All dimension is micrometer
- 2. Top view
- 3. Optical center = package center

- **Recommended Guideline for PCB Assembly**

- I. ecommended vender and type for Pb-free solder paste
 - 1 Almit LFM-48W TM-HP
 - 2 Senju M705-GRN360-K

- II. IR Reflow Soldering Profile

Temperature profile is the most important control in reflow soldering. It must be fine tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure 8 below.

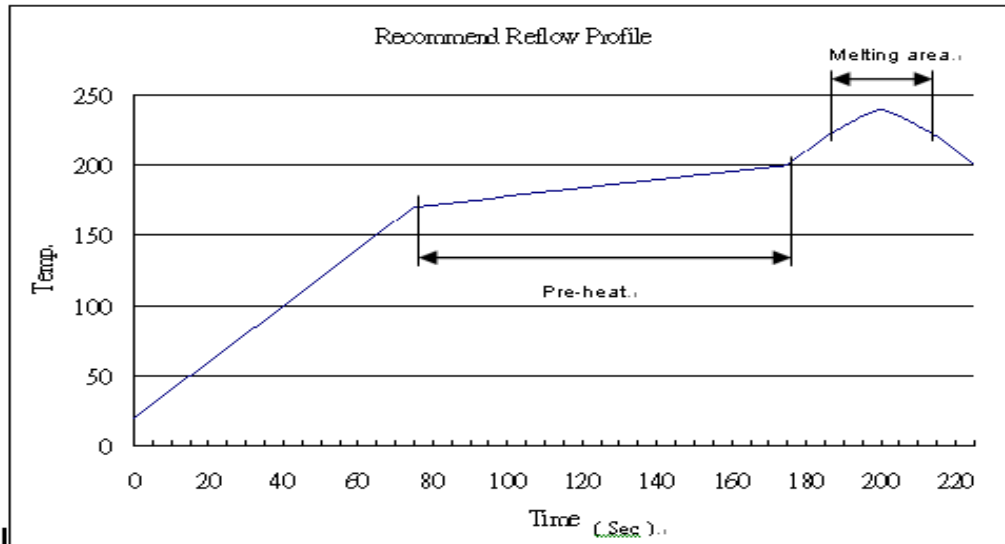


Fig.13.3 IR Reflow Profile

- **Reflow Profile**

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
 - 2.1 Temp ramp from 170~ 200 degree C
 - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
 - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
 - 3.2 Peak temperature : 245 degree C.