NTSC/PAL CMOS Image Sensor

BF3003U

Datasheet

Revised. Date	Revision	Brief Description	Author	Proofread	Authorize
A /0					

content

1. General Description

The BF3003U is a highly integrated VGA(PAL/NTSC) camera chip which includes CMOS image sensor (CIS), image signal processing function (ISP), TV-encoder and Video DAC. It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity, high dynamic range and very low power imaging system. The sensor consists of a 648×492 pixel array which has an optical format of 1/4 inch for VGA/NTSC/PAL. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, auto black level compensation, on-chip 10-bit ADC, Video encoder and on-chip Video DAC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB565, YCbCr 4:2:2, CCIR656, and support NTSC/PAL analog signal output. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor, and it also can be used as a host to control slave to set the sensor.

The product is capable of operating at up to 60 frames per second at 54MHz master clock in VGA mode and standard 576i/480i TV mode, with complete user control over image quality and data formatting. All required image processing functions, including exposure control, white balance control, color saturation control and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/4 inch for VGA/NTSC/ PAL.
- 60 frames/sec VGA mode @ 54 MHZ xclk clock.
- 60 fields/sec NTSC mode.
- 50 fields/sec PAL mode.
- Ultra-low dark noise at high temperature.
- Ultra-Low power consumption of typical 150mW@60fps, 20uA at power down.
- Ultra-Low power consumption of typical 210mW@NTSC/PAL output, 30uA at power down.
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer (648*480), CCIR656, analog NTSC/PAL .
- Power supply: 1.5V for core, 1.65V~3.6V for I/O,3.0V~3.6V for VDD3A.
- Horizontal /Vertical mirror.
- 50/60Hz flicker cancellation.
- Auto black level control.
- Image processing function: Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation and Contrast, and Data Format Conversion, Video encode, PAL/NTSC

output.

- Package: CLCC

3. Applications

- Security systems
- Automotive
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- MP4
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Industrial and environmental systems

4. Technical Specifications

- Active pixel array: 648*492
- Pixel size: 6.0um×6.0um
- Sensitivity: TBD
- Dark current: TBD at 40℃
- Power supply: 1.5/3.3V
- Power consumption: 160mW@60fps/300, 210mW@NTSC/PAL output
- Standby current: 30uA
- S/N Ratio: TBD
- Dynamic range: 65dB
- Operating temperature: -40~105℃
- Stable Image temperature -10~60℃
- Optimal lens chief ray angle: 10°
- Package: CLCC

5. Functional Overview

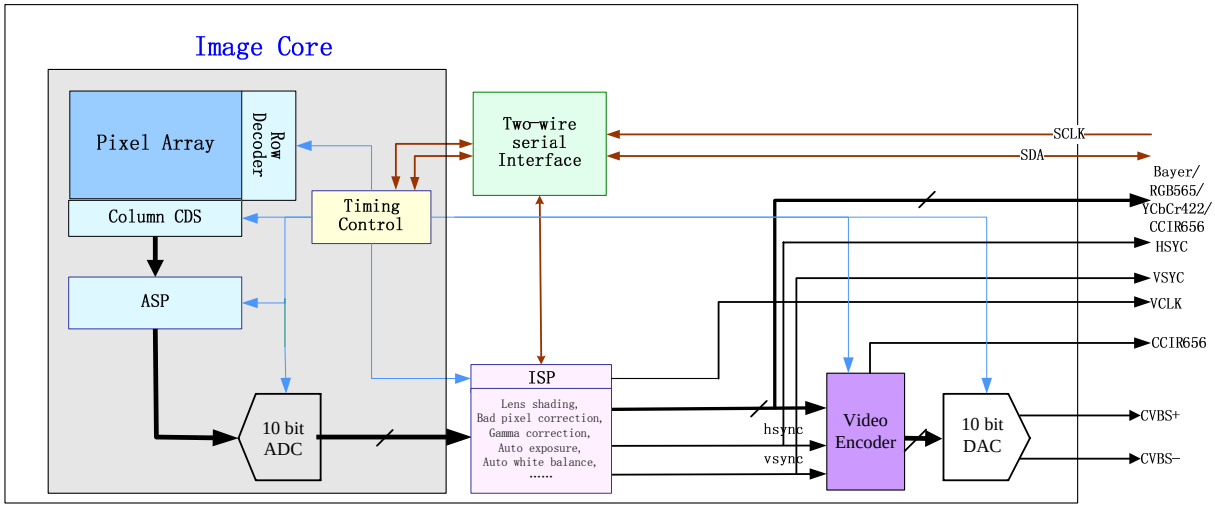

Figure 1. Block Diagram

BF3003U has an active image array of 648x492 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, color correction, gamma correction, data format conversion and so on.

BF3003U has on-chip oscillator, passive crystal can be used. For Auto., BF3003U has overlay function by via two-wire serial interface bus setting, And user can get the overlay/mirror/vflip picture by setting the I/O.

5.1 Pixel Array

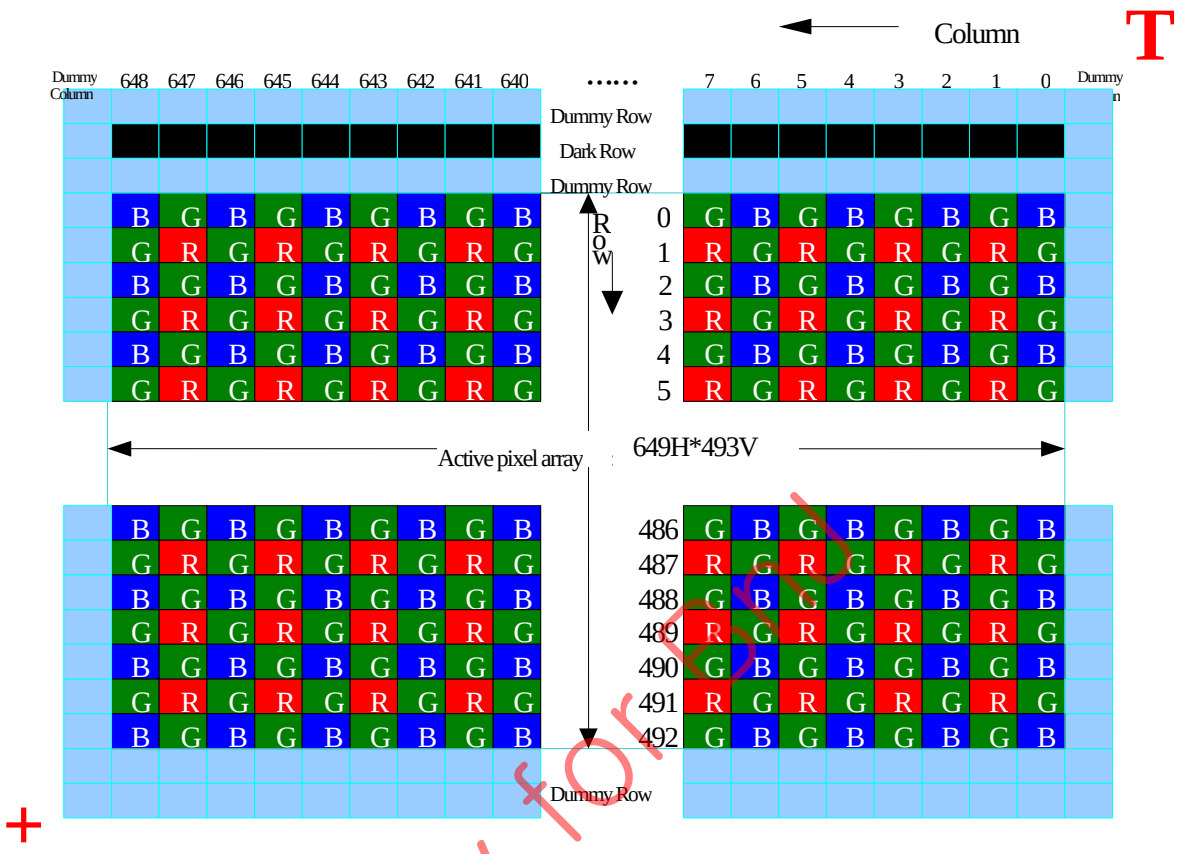

Figure 2. Sensor Array Region

The pixel array includes 649×493 effective pixels for imaging, whose address range is from (0, 0) to (648, 492). In order to improve the image uniformity, there are 2 extra dummy rows and 1 extra dark rows at the top side and 2 extra dummy rows at the bottom side of this imaging array. 1 extra dummy column is at the right.1 extra dummy columns are at the left.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF3003U can provide the Raw Bayer data, YUV data or CCIR656 data through an 8-bit output data bus. If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 648 to 1. If no flip in row, row is read out from 0 to 491. If flip in row, row is read out from 492 to 1. In this way, the output pixel color order is always the same.

Pixel array output signal order is always:

BGBGBG……

GRGRGR…..

5.2 Column CDS

BF3003U has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Timing controller

- The timing controller controls the following functions
- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- External timing outputs (VSYNC, HSYNC and VCLK)

5.4 Analog Signal Processor

This block performs all analog image functions including Color gain/Global gain control and black level compensation. Each of the R, G, B color pixel signals can be multiplied by different gain factors to balance the color of the image at various light conditions.

5.5 A/D converter

The analog signals are converted to digital forms one line at a time and data are streamed out column by column. BF3003U provides the 10-bit Raw Bayer data for ISP through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, Data Format Conversion.

5.8 Video encoder

The BF3003U has an on-chip video encoder to format the data stream for composite

video output in the supported NTSC or PAL formats. The encoder expects CCIR-656 interlaced NTSC or PAL or YUV422 data stream input,

NTSC/PAL TV standards are implemented and available as output in the BF3003U. The accuracy and stability of the crystal clock frequency is important to the TV video system. User can use a 27MHz active/passive crystal when utilizing the BF3003U camera chip.

5.9 Video DAC

BF3003U has integrated a 10bit video DAC. The digital TV signals are converted to analog forms. BF3003U provides the 10-bit on-chip video DAC to convert the TV signals for analog transfer application. The composite video output DAC is external resistor programmable and supports both single-ended and differential output. The DAC is driven by the on-chip video encoder output.

5.10 Parking line

BF3003U has integrated the parking-guide lines.
The location and color of the lines is adjustable.

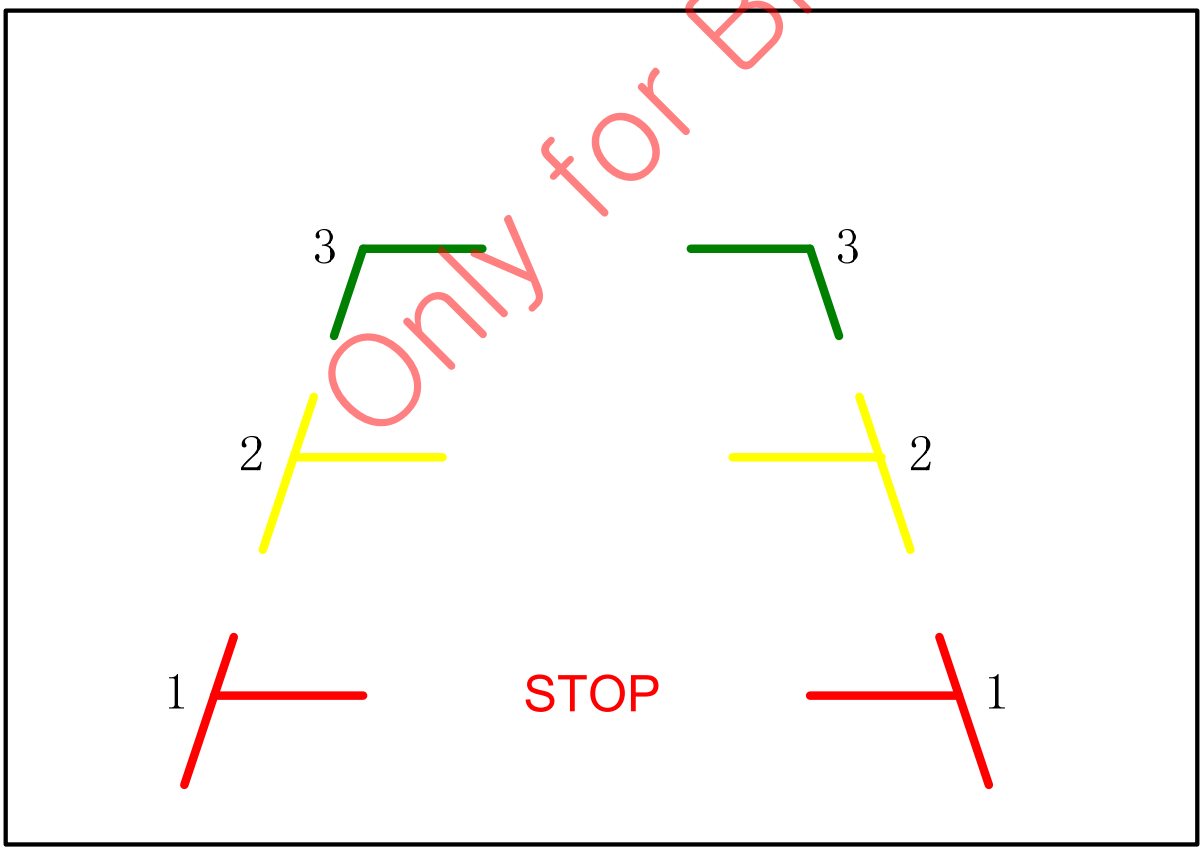

Figure 3. Parking guide line

6. Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.6 V
- Supply voltage (VDD3A): 3.0 ~ 3.6 V
- Supply voltage (VDDD): 1.35 ~ 1.65 V
- Supply voltage (VLDO): 1.65 ~ 3.6 V
- Operating temperature: -40~85 ℃
- Storage temperature: -40~125 ℃
- ESD Rating, Human Body mode: 3000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2 DC Parameters

Table 1. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	3.3	3.6	1
VDDD	Digital power supply	V	1.35	1.5	1.65	2
VLDO	LDO power supply	V	1.65	1.8 3.3	≤VDD3A	2
VDD3A	Analog power supply	V	3.0	3.3	3.6	--
VDD_DAC	DAC power supply	V	3.0	3.3	3.6	
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	8	--	
I_vddd	VDDD supply current,	mA	-- --	19	--	3
I_vldo	VLDO supply current,	mA	-- --	20	--	2
I_vdd3a	VDD3A supply current,	mA	--	30	--	3
I_vdd_dac	VDD_DAC supply current	mA	--	35	--	3

Note：

1. 1. VDDIO=3.3V （60 fps）
2. VLDO and VDDD will not be employed at the same time, and VLDO cannot be higher than VDD3A. VDDD is the supply for the core and can be generated by VLDO or by VDDD pin.
3. The Current of power is decided by the work mode, ex. Frequency of clock and output format. The Max. Current will not appear at the same time.

6.1.3 Clock Requirement

Table 2. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	--	27	--	1
MCLK	Master clock	MHz	--	54	--	2
PCLK	Pixel clock	MHZ	--	27	--	3
VCLK	Output clock	MHZ	--	27	--	4
SCLk	two-wire serial interface clock frequency	KHz	--	400	--	5

Note:

1. XCLK is the input clock and it is the input of PLL.
2. MCLK is the master clock of the system, and it can be generated by PLL.
3. PCLK is the pixel clock and its frequency is half of MCLK's.
4. VCLK is the output clock of the system.
5. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section

6.2 Electro-Optical Characteristics

Clock frequency: 27MHz.
Operating voltage: VDDIO=3.3V, VDDD=1.5V, VDD3A=3.3V.
Operating temperature: 25°C

Table 3. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	–	TBD		1
Dark current	mV/sec	–	TBD	–	2
S/N ratio	dB	–	TBD	–	–
Dynamic Range	dB	–	TBD	–	–
Frame Rate	fps	–	30	60	3

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (40 Celsius).
3. With 640×480 window size at MCLK 54MHz.

6.3 Timing

6.3.1 The Sensor-core Readout Mode

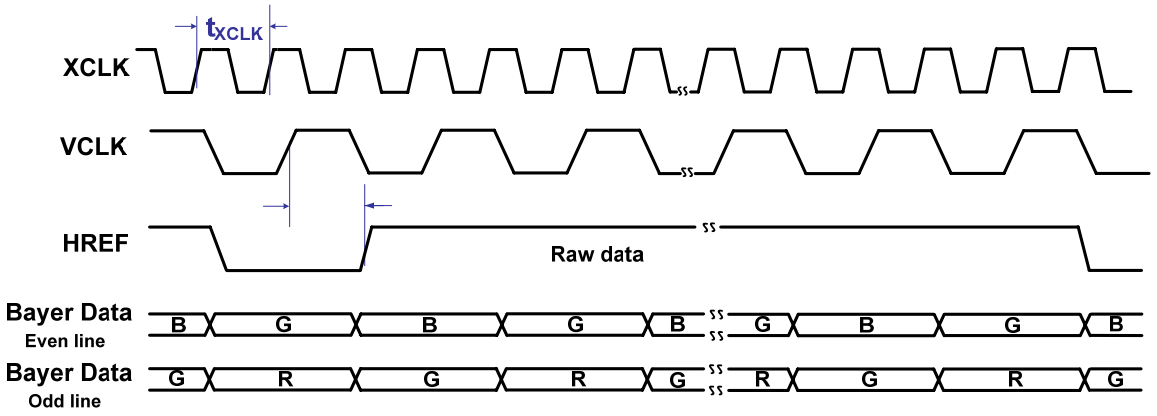

Figure 4. Horizontal Timing Raw Bayer Data

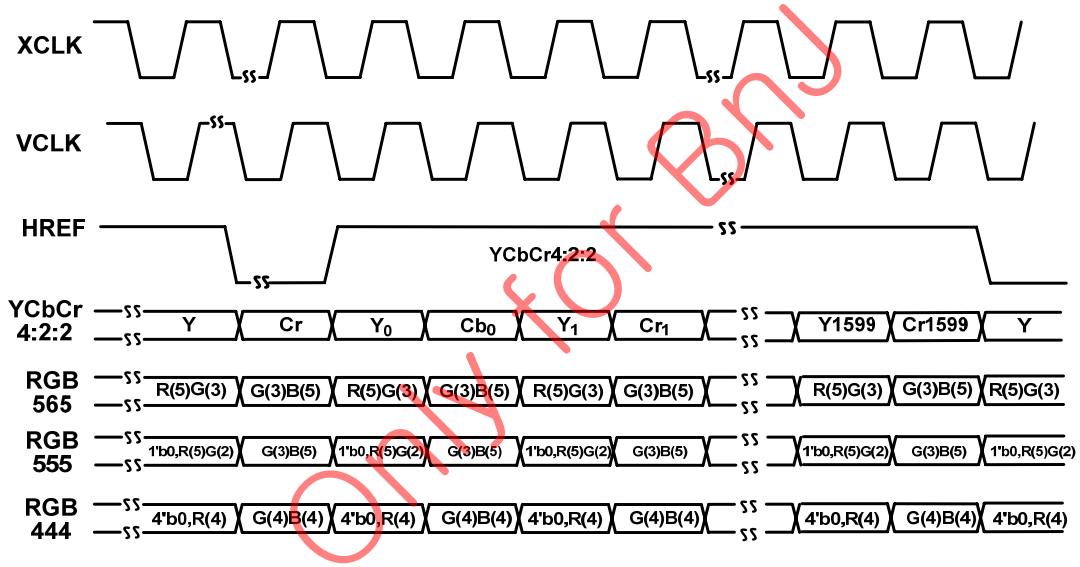

Figure 5. Horizontal Timing YUV4:2:2

Table 4. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	t_P=2 x t_{MCLK}	–	37	–	ns
f_{MCLK}	Master Clock Frequency	–	54	–	MHz
f_{VCLK}	Video Clock Frequency for Raw data , fV= $f_{MCLK/2}$ for YUV/RGB , fV= f_{MCLK}	–	27/54	–	MHz
t_{LINE}	Line length	–	864x t_P	–	ns
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	–	–	us
t_{HIGH}	Clock High Period	600	–	–	ns
$t_{HD:STA}$	Start condition Hold Time	600	–	–	ns
$t_{SU:STA}$	Start condition Setup Time	600	–	–	ns
$t_{HD:DAT}$	Data-in Hold Time	0	–	–	ns

Symbol	Descriptions	Min.	Typ.	Max.	Unit
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

6.3.2 The PAL Mode Timing

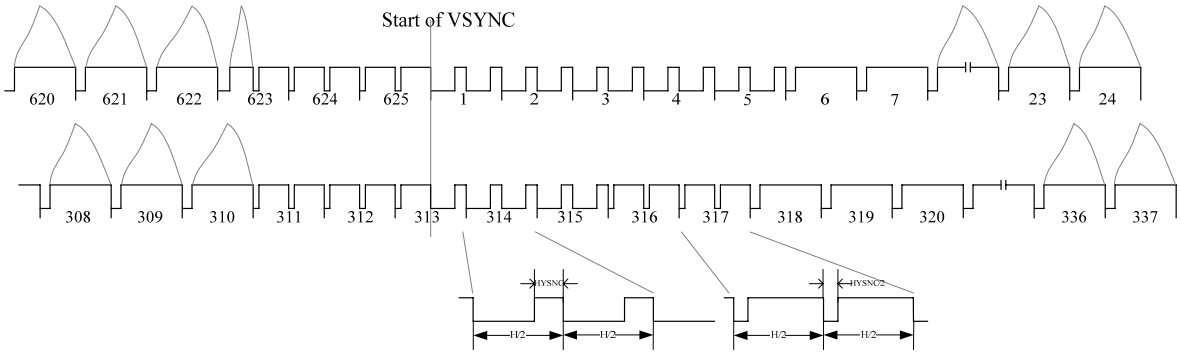

Figure 6. PAL Vertical Interval Timing

6.3.3 The NTSC Mode Timing

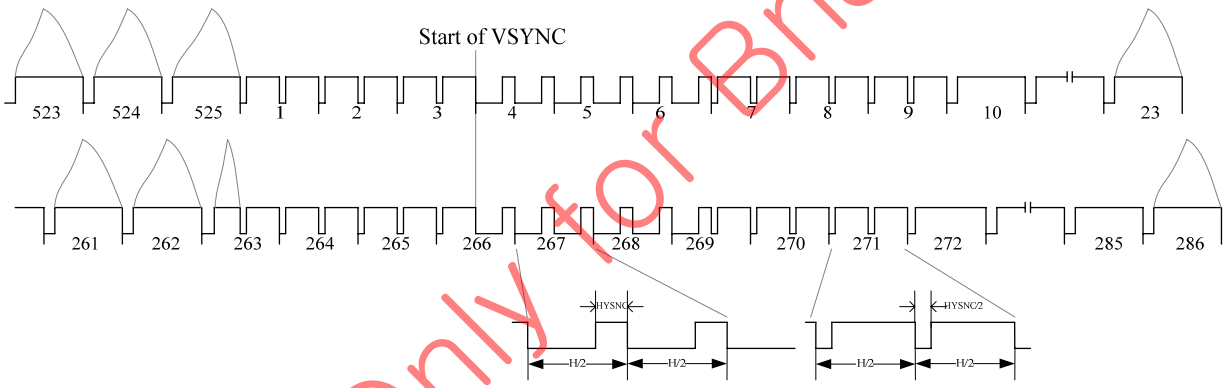

Figure 7. NTSC Vertical Interval Timing

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

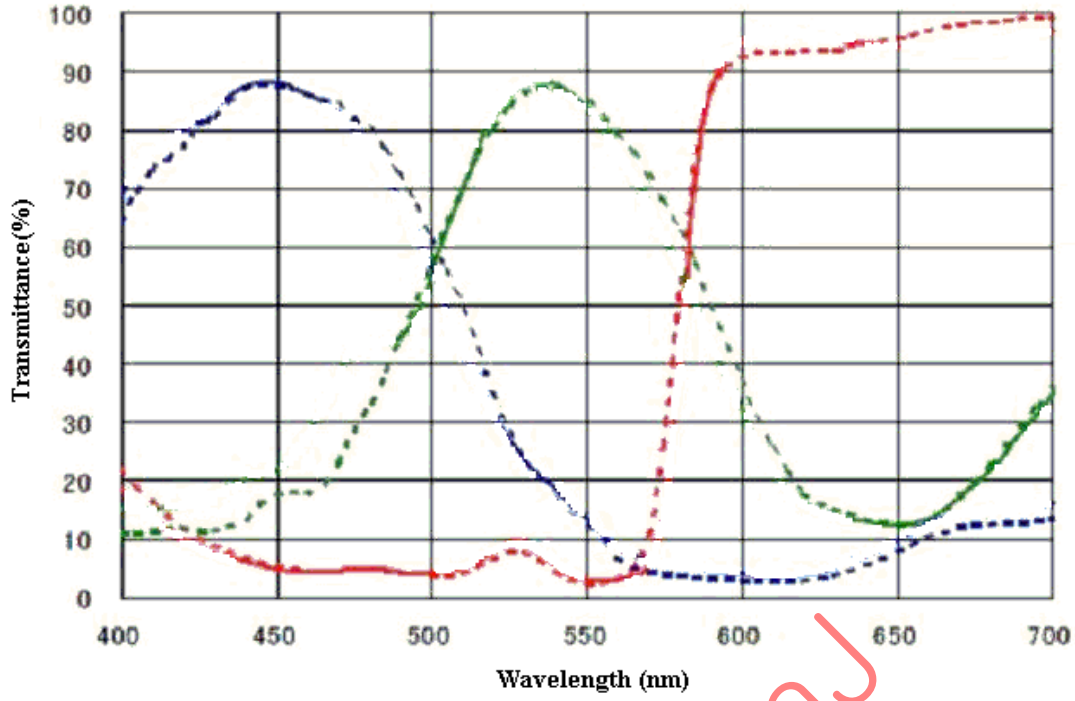

Figure 8. Spectral Characteristics

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF3003U are written and read through the two-wire serial interface. BF3003U has two-wire serial interface slave and master. BF3003U is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF3003U through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF3003U is 7'b1101110 (0X6e).

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF3003U uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 The Two-wire Serial Interface Timing

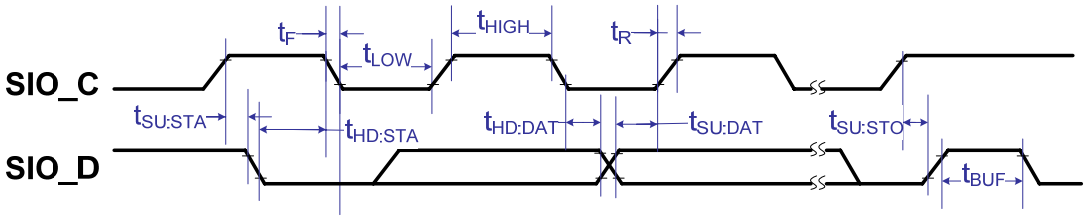

Figure 9. Two-Wire Serial Interface Timing

7.3 Two-wire Serial Interface Functional Description

Single Write Mode Operation

S	Slave address	W	A	Register address	A	Data	A	P

Multiple Write Mode (Register address is increased automatically)[1] operation

S	Slave address	W	A	Register address	A	Data	A	. . .

. . .	A	Data	A	Data	A	. . .	A	Data	A	P

Single Read Mode Operation

S	Slave address	W	A	Register address	A	. . .

Sr	Slave address	R	A	Data	NA	P

Multiple Read Mode (Register address is increased automatically)[1] Operation

S	Slave address	W	A	Register address	A	. . .

Sr	Slave address	R	A	Data	A	Data	A	. . .

. . .	A	Data	A	Data	NA	P

From master to slave From slave to master

S: Start condition. Sr: Repeated Start (Start without preceding stop.)

Slave Address:

write address = DCh = 11011100b

read address = DDh = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit. NA: No Acknowledge.
Data: 8-bit data P: Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.4 The Two-wire Serial Interface master

Connect external Two-wire Serial Interface slave-compatible storage device through the BF3003U Two-wire Serial Interface master interface, so the BF3003U can self load the configuration data from it. Data stored in the external storage device should be arranged as follows:

Address	Value
0x00	The number of the register must be written.
0x01	Addr1—The first configuration register address.
0x02	Addr1_value—The first configuration register value.
0x03	Addr2—The second configuration register address.
0x04	Addr2_value—The second configuration register value.
…	…

7.5 Register Summary (full list)

Table 5. BF3003U all registers

Address	Name	Width	Default value	Description
00h	***DBLKHE***	6	20h	Reserved
01h	***BLUE_GAIN***	6	19h	blue gain register
02h	***RED_GAIN***	6	15h	red gain register
03h	***VHREF***	8	00h	Bit[7:6]: VREF end low 2 bits(high 8 bits at VSTOP[7:0]) Bit[5:4]: VREF start low 2 bits(high 8 bits at VSTART[7:0]) Bit[3:2]: HREF end low 2 bits(high 8 bits at HSTOP[7:0]) Bit[1:0]: HREF start low 2 bits(high 8 bits at HSTART[7:0])
04h	***Total_Row_D***	8	78h	Reserved
05h	***LOFFN1E***	6	1eh	Coarse negative offset control-even col.
06h	***LOFFN0E***	6	20h	Fine negative offset control- even col.
07h	***KDC_CNTL***	8	00h	Reserved
08h	***LOFFN0O***	6	20h	Fine negative offset control- odd col.
09h	***COM2***	8	00h	Bit[7:6]: Vclk output drive capability 00:1x 01:1.5x 10:2.5x 11:3x Bit[5]: Tri-state option for output data at power down period 0:tri-state at this period 1:No tri-state at this period Bit[4]: Tri-state option for output clock at power down period 0:tri-state at this period

Address	Name	Width	Default value	Description
				1:No tri-state at this period Bit[3:2]: hsync output drive capability 00:1x 01:1.5x 10:2.5x 11:3x when drivesel=0 Bit[1:0]: data&clk&Hsync output drive capability 00:1x 01:1.5x 10:2.5x 11:3x when drivesel=1 Bit[1:0]: data output drive capability 00:1x 01:1.5x 10:2.5x 11:3x
0ah	***L_EN,INT_TIM_TH***	8	a0h	Reserved
0bh	***S_EN,OFFSET_TH***	8	9ch	Reserved
0ch	***COM3***	8	00h	Bit[7]:PROCRSS RAW selection 0: process raw from ycbcr to rgb conversion in datformat 1: process raw from color interpolation(deniose,gamma,lsc is selectable) Bit[6]:Output data MSB and LSB swap Bit[5:4]:PROCESS RAW sequence(when 0x0c[7]=0): 00: (LINE0:BGBG/LINE1:GRGR) 01: (LINE0:GBGB/LINE1:RGRG) 10: (LINE0:GRGR/LINE1:BGBG) 11: (LINE0:RGRG/LINE1:GBGB) Bit[3]:0:no HREF when VSYNC_DAT=0; 1:always has HREF no matter VSYNC_DAT=0 or not; Bit[2]:DATA ahead 1 clk(YUV MCLK,RawData PCLK) or not Bit[1]:HREF ahead 1 clk(YUV MCLK,RawData PCLK) or not Bit[0]:HREF ahead 0.5 clk(YUV MCLK,RawData PCLK) or not 0x0c[1:0]: Reserved
0dh	***DBLKLE***	6	20h	I Reserved
0eh	***DBLKHO***	6	20h	I Reserved
0fh	***DBLKLO***	6	20h	Reserved
10h	***INT_TIM_TH***	8	50h	Reserved
11h	***CLKRC***	8	00h	B Bit[7：2]: Reserved Bit[1:0]:Internal MCLK pre-scalar 00:divided by 1 F(MCLK)=F(pll output clock) 01:divided by 2 F(MCLK)=F(pll output clock)/2 10:divided by 4 F(MCLK)=F(pll output clock)/4 11: no clocking, digital stand by mode(all clocks freeze)
12h	***COM7***	8	00h	Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Reserved Bit[5]: (when 0x4a =03h)0: row 1/2 sub,1: output input image. Bit[4]: 1/2 digital subsample Selection(only for YUV422/RGB565/RGB555/RGB444 output). Bit[3]: data selection 0:normal(YUV422/RGB565/RGB555/RGB444/BAYER RAW/PRO RAW) 1:CCIR656 output enable(for TV) Bit[2]: YUV422/RGB565/RGB555/RGB444 Selection. Bit[1]: Reserved. Bit[0]: Raw RGB Selection. {0x12[2],0x12[0]} 00: YUV422 01: Bayer RAW 10: RGB565/RGB555/RGB444(use with 0x3a) 11: Process RAW(use with 0x0c[7])

Address	Name	Width	Default value	Description
13h	***COM8***	8	17h	Bit[7:6]: Reserved Bit[5:4]：Reserved Bit[3]: Reserved Bit[2]: AGC Enable for long int_tim. 0:OFF , 1: ON. Bit[1]: AWB Enable. 0:OFF , 1: ON. Bit[0]: AEC Enable for long int_tim. 0:OFF , 1: ON.
14h	***LOFFN1O***	6	1eh	Reserved
15h	***COM10***	8	02h	Bit[7]: Reserved Bit[6]: 0:HREF, 1:HSYNC Bit[5]: 0:VSYNC_IMAGE, 1:VSYNC_DAT Bit[4]: VCLK reverse Bit[3]: HREF option, 0:active high, 1:active low. Bit[2]: Reserved Bit[1]: VSYNC option, 0:active low, 1:active high. Bit[0]: HSYNC option, 0:active high, 1:active low.
16h	***BIAS2***	8	02h	Reserved
17h	***HSTART***	8	00h	Output Format-Horizontal Frame(HREF column)start high 8-bit(low 2bits are at VHREF[1:0])
18h	***HSTOP***	8	a0h	Output Format-Horizontal Frame(HREF column)end high 8-bit(low 2 bits are at VHREF[3:2])
19h	***VSTART***	8	00h	Output Format-Vertical Frame(row)start high 8-Bit(low 2 bits are at VHREF[5:4])
1ah	***VSTOP***	8	78h	Output Format-Vertical Frame(row)end high 8-Bit(low 2 bits are at VHREF[7:6])
1bh	***PLLCTL***	8	80h	PLLCTL[7]: PLL Enable 0:enable 1:disable PLLCTL[6:0]: Reserved
1ch	***Win_P2_Y***	8	82h	Reserved
1dh	***Win_P2_X***	8	46h	Reserved
1eh	***MVFP***	8	00h	Bit[7:6]: Reserved Bit[5]: Mirror(0:Normal image 1:Mirror image) Bit[4]: Vflip enable(0:Normal image 1:Vertically flip) Bit[3:0]: Reserved
1fh	***DBLK_TARO***	8	20h	Black control target for odd col
20h	***TDREG***	8	80h	Reserved
21h	***TAREG***	8	00h	Reserved
22h	***DBLK_TARE***	8	20h	Black control target for even col
23h	***GLGAINREG***	7	55h	GreenGain[2:0] for high sensitivity: bit[2:0]: for odd column (used as GreenOgain[2:0]) bit[6:4]: for even column (used as GreenEgain[2:0])
24h	***TAR_NORMAL***	8	82h	Y target value1 for normal mode .
25h	***AE_LOC***	8	88h	Reserved
26h	***STEPE***	8	44h	Reserved
27h	***STEPO***	8	44h	Reserved
28h	***DBLK_CNTL***	7	44h	Reserved
29h	***BIAS1***	8	00h	Reserved
2ah	***EXHCH& NULL_MAKEUP_RST_CNTL & DOUBLE_RESET_CNTL & HDR_M_B_SEL***	8	0eh	Bit[7:4]: 4MSB for dummy pixel insert in horizontal direction Bit[3:0]: Reserved
2bh	***EXHCL***	8	00h	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2ch	***DREF2***	8	00h	Reserved

Address	Name	Width	Default value	Description
2dh	***DIG_GAIN_MAX(write) & DIG_GAIN(read)***	8	54h	contorl high bright Y value limit,and DIG_GAIN. DIG_GAIN_MAX[7:4] is the bit[7:4] of high bright Y value limit. When DIG_GAIN_MAX[7:4] > DIG_GAIN_MAX[3:0] ,{DIG_GAIN_MAX[3:0],4'b0} is the MAX value of DIG_GAIN.
2eh	***HDR_ENABLE SENSITIVITY BW_CONTROL***	8	15h	Bit[7:6]: Reserved Bit[5:4]:BW_CONTROL[5:4] 2'b0x- do the black_white mode automaticily. 2'b10- show colorized. 2'b11- show black and white. Bit [3:0]:the gain bound when BW switch.
2fh	***DREF***	8	8ch	Reserved
30h	***HSYST***	8	aeh	control the rising edged of HSYNC[7:0]
31h	***HSYEN***	8	12h	control the falling edged of HSYNC[7:0]
33h	***OFFSET_MODE***	8	00h	Lens shading offset selection. Bit[7] 0: use black_aver as offset 1: use register OFFSET_REG as offset Bit[6:0] black_aver(readonly)
34h	***OFFSET_REG***	8	38h	lens shading offset(reg)
35h	***R_COEF***	8	46h	lens shading gain of R
36h	***L_PASS,S_PASS Y0_H,X0_H***	8	01h	bit[7:6] : Reserved bit[4] Center Y coordinate MSB bit[0] Center X coordinate MSB
37h	***Y0_L***	8	f7h	Center Y coordinate LSB
38h	***X0_L***	8	45h	Center X coordinate LSB
39h	***OFFSET2***	8	80h	GammaOffset2: bit[7]: 0:positive ,1:negative bit[6:0] : value

3ah	***TSLB***	8	00h	if YUV422 is selected, the Sequence is:
				Bit[1:0]:Output YUV422 Sequence
				00: YUYV, 01: YVYU
				10: UYVY, 11: VYUY
				if RGB565/RGB555/RGB444 is selected, the Sequence is:
				Bit[4:0]:Output RGB565/RGB555/RGB444 Sequence
				RGB565:
				00h: R5G3H,G3LB5 01h: B5G3H,G3LR5
				02h: B5R3H,R2LG6 03h: R5B3H,B2LG6
				04h: G3HB5,R5G3L 05h: G3LB5,R5G3H
				06h: G3HR5,B5G3L 07h: G3LR5,B5G3H
				08h: G6B2H,B3LR5 09h: G6R2H,R3LB5
				RGB555:
				0Ah: 1'b0R5G2H,G3LB5 0Bh: G3LB5,1'b0R5G2H
				0Ch: R5G3H,G2LB51'b0 0Dh: G2LB51'b0, R5G3H
				0Eh: B5G3H,G2L1'b0,R5 0Fh: R5G3H,G2L1'b0,B5
				10h: B51'b0G2H,G3LR5 11h: R51'b0G2H,G3LB5
				RGB444:
				12h: 4'b0R4,G4B4 13h: G4B4,4'b0R4
				14h: 4'b0B4,G4R4 15h: G4R4,4'b0B4
				16h: R4G4,B44'b0 17h: B44'b0,R4G4
				18h: B4G4,R44'b0 19h: R44'b0,B4G4
				1Ah: B4G4,R4B4 1Bh: R4G4,B4R4
				1Ch: R4G2H2'b0,G2LB42'b0 1Dh: B4G2H2'b0,G2LR42'b0
				1Eh: B41'b0G3H,G1L2'b0R41'b0 1Fh: R41'b0G3H,G1L2'b0B41'b0

3bh	***LS_SEL,Y_AVER_TH***	8	60h	Reserved
3ch	***TDACREG***	8	08h	Reserved
3dh	***DREF1***	8	00h	Reserved

Address	Name	Width	Default value	Description
3eh	***ADD_EN,OFFSET_TH2***	8	a4h	Bit[7] ADD_EN ,if ADD_EN=1'b1,compensate (Din-OFFSET),else don't compensate (Din-OFFSET);Bit[6:0] OFFSET_TH2 when current Y_AVER<Y_AVER_TH, OFFSET1-OFFSET_TH2*X/4 will be used for auto offset adjust.
3fh	***OFFSET1***	8	9ah	GammaOffset1: bit[7] 0: use black_aver as offset 1: use register OFFSET1[6:0] as offset
40h	***k0***	8	28h	Gamma Correction Slop Coefficients
41h	***k1***	8	28h	Gamma Correction Slop Coefficients
42h	***k2***	8	30h	Gamma Correction Slop Coefficients
43h	***k3***	8	29h	Gamma Correction Slop Coefficients
44h	***k4***	8	23h	Gamma Correction Slop Coefficients
45h	***k5***	8	1bh	Gamma Correction Slop Coefficients
46h	***k6***	8	17h	Gamma Correction Slop Coefficients
47h	***k7***	8	0fh	Gamma Correction Slop Coefficients
48h	***k8***	8	0ch	Gamma Correction Slop Coefficients
49h	***k9***	8	0bh	Gamma Correction Slop Coefficients
4ah	***SUBSAMPLE & HDR_CHG_CNT & TX2_SEL & HREF_CNTL***	8	a6h	Bit[7:0]: Reserved;
4bh	***k10***	8	09h	Gamma Correction Slop Coefficients
4ch	***k11***	8	08h	Gamma Correction Slop Coefficients
4dh	***DATA_COE(write) & Coe_S(read)***	8	3ch	Reserved
4eh	***k12***	8	07h	Gamma Correction Slop Coefficients
4fh	***k13***	8	05h	Gamma Correction Slop Coefficients
50h	***k14***	8	04h	Gamma Correction Slop Coefficients
51h	***target2***	8	93h	Color Correction Coefficients
52h	***target3***	8	04h	Color Correction Coefficients
53h	***target4***	8	87h	Color Correction Coefficients
54h	***target6***	8	88h	Color Correction Coefficients
55h	***BRIGHT***	8	00h	Brightness control: bit[7] : 0:positive ,1:negative bit[6:0] : value
56h	***Y_COEF***	8	40h	Y Coefficient for Contrast
57h	***target7***	8	82h	Color Correction Coefficients
58h	***target8***	8	8dh	Color Correction Coefficients
59h	***TARGET_ADJ***	4	eh	Bit[3:0]:color martrix adjust coefficient,used when the current GLB_GAIN>2*0x5a[5:0], smaller value is for larger adjust.
5ah	***GLB_GAIN_THD***	6	18h	Bit[5:0]:2*Bit[5:0] is used as glb_gain threshold for color martrix adjust, smaller value is for larger adjust.
5bh	***P_TH***	8	4ch	skin probability threshold
5ch	***SKIN_CTR***	4	0bh	bit[7:4]: Reserved bit[3]: 0:disable skin function 1:enable skin function bit[2]: 0:disable hue rotate 1:enable hue rotate bit[1]: 0:display full resolution and can do hue full resolution 1:only can do hue within skin area (use with 0xef[0]) bit[0]: when 0xef[1]=1'b1, 0: only display skin area,others black,and only can do hue within skin area 1:display full resolution and only can do hue within skin area when 0xef[1]=1'b0,0、1:display full resolution and can do hue full resolution

Address	Name	Width	Default value	Description
5eh	***SHORT_SEL***	8	00h	Reserved
5fh	***DATA_MAX(write) & Min_front(read)***	8	00h	data max manual
60h	***HDRCTR***	8	11h	Reserved
61h	***SCALE_SEL(write) & B_S_FRONT(read)***	8	20h	Reserved
62h	***OFF_TH_S(write) & Max_front(read)***	8	10h	Reserved
64h	***DREF3***	8	00h	Bit[7:0]:Reserved
65h	***G_COEF***	8	46h	lens shading gain of G
66h	***B_COEF***	8	46h	lens shading gain of B
67h	***MANU***	8	80h	Manual U value
68h	***MANV***	8	80h	Manual V value
69h	***DICOM1***	8	80h	Bit[7]: YCBCR RANGE select 0: YCBCR 0~255 1: Y 16~235, CBCR 16~240 Bit[6]: Negative image enable 0: Normal image, 1: Negative image Bit[5]: UV output value select. 0: output normal value 1: output fixed value set in MANU and MANV Bit[4]:U、V dither when ycbcr mode/R、B dither when rgb mode: 0: low 2 bits, 1: low 3bits Bit[3]:Y dither when ycbcr mode/G dither when rgb mode: 0: low 2 bits, 1: low 3bits Bit[2]:Y dither enable Bit[1]:U、V dither enable Bit[0]:RGB dither enable
6ah	***DE_GAIN_EN & LS_GNGAINREG & GNGAINREG***	8	91h	Reserved
6ch	***CLKDIV***	8	80h	Reserved
6dh	***AVER_E***	8	RO	Reserved
6eh	***AVER_O***	8	RO	Reserved
6fh	***DICOM2***	8	20h	Bit[7]: 0: enable PRE_DATFOR, 1: bypass PRE_DATFOR Bit[6:0]:Y threshold for dither, dither is only enable for the pixel: Y<2*DICOM2[6:0].
70h	***IntCtr***	8	afh	BIT[7:6]:Edge_Gain_P: positive edge enhancement gain: 00:0.5, 01:1.0, 10:1.5, 11:2.0; BIT[5:4]:Edge_Gain_N: negative edge enhancement gain: 00:0.5, 01:1.0, 10:1.5, 11:2.0; BIT[3]:edge_switch–edge enhancement enable 1'b0:disable 1'b1:enable BIT[2]:raw_Switch–processed rawdata output format: (use with 0x0c[7]=1) 1'b0:648x488 1'b1:652x492 BIT[1]:Bp_switch–bad pixel's correction 1'b0:disable 1'b1:enable BIT[0]:Lpf_switch–low pass filter 1'b0:disable 1'b1:enable
71h	***BpcCtr***	8	a6h	Reserved
72h	***DenCtr***	8	1fh	Reserved
73h	***EdgCtr***	8	2fh	Reserved

Address	Name	Width	Default value	Description
74h	*DaeCtr*	8	2ah	Reserved
75h	*DakCtr*	8	83h	Reserved
76h	*ColCtr*	8	9eh	Reserved
77h	*EffCtr*	8	00h	Reserved
78h	*SobCtr*	8	15h	Reserved
79h	*SobMax*	8	55h	Reserved
7ah	*MacCtr*	8	cfh	Reserved
7bh	*MacTh*	8	e3h	Reserved
7ch	*Mot_Th*	8	1eh	BIT[7:0]: Threshold for motion detection
7dh	*Mot_LE*	8	01h	Reserved
7eh	*Mot_Ctrl*	8	99h	Reserved
7fh	*Win_P1_X*	8	32h	BIT[7:0]: the column number of the upper-left point of the customer specified window(*2)
80h	*AE_MODE*	8	92h	Bit[7]:AE adjust control, 1:AE adjust auto ; 0:when AE_MODE[0] = 0 , AE adjust manual. Bit[6]: 0 : AE adjusts every two frames ; 1: AE adjusts every frame when Y_DIFF_D[6:3] > TAR_BASE[7:4] and normal mode. Bit[5:4]:G_MIN_SLOPE When INT_TIM >INT_MID ,gain Coefficients. 2'b00: 0 ; 2'b01: 1; 2'b10:2; 2'b11: 3. Bit[3]:DIG_GAIN limit enable. 1:enable; 0:diaable. Bit[2]:Tar_OFF Coefficient , for adjust dig_gain speed. Bit[1]:0:choose 60HZ step ,1:choose 50HZ step. Bit[0]: STEPS_EN when STEPS_EN chages,and Bit[7] is zero，AE is adjusted manual。
81h	*AE_SPEED*	8	00h	Bit[7:4] : the speed of adjusting from light to dark Bit[3:0] : the speed of adjusting from dark to light
82h	*GLB_MIND1(write) & P_PIXEL_OE(read)*	8	12h	Reserved
83h	*GLB_MAXD1(write) & Y_AVER_MODIFY(read)*	8	2ch	Reserved
84h	*GLB_MIND2*	8	2ch	Reserved
85h	*GLB_MAXD2*	8	40h	Reserved
86h	*GLB_MAXD3*	8	1bh	Reserved
87h	*GLB_L_GAIN0/ GLB_S_GAIN0 TAR_BASE1*	8	66h	Reserved
88h	*Y_READ TAR_BASE2*	8	a0h	Reserved
89h	*INT_MAX_MID*	8	7d	bit[2:0]:INT_MID ; bit[7:3]:INT_MAX.
8ah	*INT_STEP_50*	8	36h	50HZ Banding Filter STEP low 8 bits, bit[8] is in 0x96[4]
8bh	*INT_STEP_60*	8	04h	60HZ Banding Filter STEP low 8 bits, bit[8] is in 0x96[5]
8ch	*INT_TIM_L[15:8]*	8	01h	when read , the int_tim MSB output ; when write , the int_tim MSB write in.
8dh	*INT_TIM_L[7:0]*	8	36h	when read , the int_tim LSB output ; when write , the int_tim LSB write in.
8eh	*COM2*	8	36h	Reserved
8fh	*TAR_HDR_L*	8	82h	Reserved
90h	*REGISTER1*	8	90h	Reserved

Address	Name	Width	Default value	Description
91h	*Y_HDR_TH_H*	8	f0h	Reserved
92h	*INT_TIME_CH*	8	bch	Reserved
93h	*INT_MIN*	8	81h	bit[7]: 0 :INT_MIN is step ;1:INT_MIN is bit[6:0]
94h	*TAR_BASE0*	8	02h	TAR_BASE0[7:4] is used to adjust the speed of AE; TAR_BASE0[3:0] is used to control the bound of AE,the bound is 4 mult .
95h	*GLB_HIGH*	8	10h	Reserved
96h	*GLB_MAXS3*	8	ffh	Reserved
97h	*GLB_S_GAIN1*	8	12h	Reserved
98h	*COM1*	8	02h	Bit[7:3]: Reserved Bit[2:0]:weight select: weight_sel region1 region2 region3 region4 000: 1/4 1/4 1/4 1/4 001: 1/2 1/4 1/8 1/8 010: 5/8 1/8 1/8 1/8 011: 3/8 3/8 1/8 1/8 100: 3/4 1/4 0 0 101: 5/8 3/8 0 0 110: 1/2 1/2 0 0 111: 1 0 0 0
99h	*GLB_L_GAIN1*	8	1ch	Reserved
9ah	*GLB_GAIN_CHD*	8	12h	Reserved
9bh	*GLB_GAIN_CHD1*	8	48h	Reserved
9ch	*GLB_GAIN_CHD2*	8	24h	Reserved
9dh	*INT_S_IN/ INT_TIM_S*	8	8bh	Reserved
9eh	*BW_GAIN_TH*	8	36h	Reserved
9fh	*TAR_HDR_S*	8	82h	Reserved
a0h	*AWB_CTR_SET*	8	d0h	bit[7]:For manual write RGAIN/BGAIN mode: 0:RGAIN/BGAIN can't be writed if AWB_EN=0 not strides over vsync's negedge 1:RGAIN/BGAIN can be writed no matter AWB_EN=0 strides over vsync's negedge or not bit[6]:0:select the pixels wiped off gain's infection to do white balance 1:select the pixels not wiped off gain's infection to do white balance bit[5]:0:when r_aver>g_aver&&r_gain>g_gain_base or r_aver<g_aver&&r_gain<g_gain_base and |r_aver-g_aver|>limit, select r wiped off gain's infection to do white balance,the same to b; 1:select the pixels not wiped off gain's infection to do white balance bit[4]:0:select the pixels not wiped off gain's infection to do white balance 1:when white pixel amount doesn't achieve the limit,select the pixels wiped off gain's infection to do white balance bit[3]:single step debug bit[2]:single step debug enable bit[1:0]: 00:read out r_aver 01:read out g_aver 10:read out b_aver 11:read out g_aver
a1h	*AWB_TH1_SET*	7	31h	bit[6:4]:Auto White Balance Lock Boundary bit[3:0]:AWB Update Speed
a2h	*BLU_GAIN_TH1*	6	0bh	bit[5:0]The threshold of blue_gain_low

Address	Name	Width	Default value	Description
a3h	***BLU_GAIN_TH2***	6	3fh	bit[5:0]The threshold of blue_gain_high
a4h	***RED_GAIN_TH1***	6	09h	bit[5:0]The threshold of red_gain_low
a5h	***RED_GAIN_TH2***	6	3fh	bit[5:0]The threshold of red_gain_high
a6h	***COUNT_EN***	8	04h	AWB criterion : white pixels count threthold, '1' equal to 1024 pixels.
a7h	***BASE_B_GAIN***	8	a5h	bit[4:0]:base B gain for high sensitivity
a8h	***BASE_R_GAIN***	8	1ah	bit[4:0]:base R gain for high sensitivity
a9h	***AWB_CB_LIM***	8	52h	AWB criterion :CB
aah	***AWB_CR_LIM***	8	52h	AWB criterion :CR
abh	***AWB_BR_LIM***	8	18h	AWB criterion :CBCR
ach	***AWB_Y_LOW***	8	3ch	AWB criterion :Y_LOW
adh	***AWB_Y_HIG***	8	f0h	AWB criterion :Y_HIGH
aeh	***SKIN_TH_SET***	8	57h	Reserved
afh	***RGB_AVER***	8	ro	Reserved
b0h	***SAT_CTR1***	8	94h	saturation control: Bit[7] saturation mode 0:normal 1:auto. Bit[6] 0:Yavaer threshold lock is +/-4, 1:Yavaer threshold lock is +/-7; Bit[5:0] 2*SAT_CTR1[5:0] is used as Ypixel threshold for auto saturation(for dark region); larger value is for larger adjust.
b1h	***CB_COEF***	8	c6h	Cb Coefficient for Color Saturation
b2h	***CR_COEF***	8	cch	Cr Coefficient for Color Saturation
b3h	***SAT_CTR2***	8	84h	Bit[7:4]:16*SAT_CTR2[7:4] is used as Yavaer threshold for auto saturation. Bit[3:0]: 2*SAT_CTR2[3:0] is used as Cb、Cr threshold for auto Saturation (for gray region); larger value is for larger adjust.
b4h	***ECMDA***	8	13h	bit[7:0] Reserved
b5h	***ECMDB***	8	10h	bit[7:0] Reserved
b6h	***MAN_R***	8	80h	define R value
b7h	***MAN_G***	8	80h	define G value
b8h	***MAN_B***	8	80h	define B value
b9h	***TEST_MODE***	8	00h	8'h00 :normal output; 8'h01~8'h0f:overlay vertical bar patternpattern ; 8'h10~8'h1f:overlay horizontal bar pattern ; 8'h20~8'h2f:overlay vertical gradual pattern ; 8'h30~8'h3f:overlay horizontal gradual pattern ; 8'h40~8'h5f:overlay manual pattern ; 8'h60~8'h7f:overlay auto scan mode ; 8'h80~8'h8f:fixed vertical bar patternpattern ; 8'h90~8'h9f:fixed horizontal bar pattern ; 8'ha0~8'haf:fixed vertical gradual pattern ; 8'hb0~8'hbf:fixed horizontal gradual pattern ; 8'hc0~8'hdf:fixed manual pattern ; 8'he0~8'hff:fixed auto scan mode ;
bah	***ESAT***	8	00h	Reserved
bbh	***ECONT***	8	00h	Reserved
bch	***BRIGHT***	8	00h	Reserved
bdh	***FSC_ADJM***	8	00h	Reserved
beh	***FSC_ADJL***	8	00h	Reserved

Address	Name	Width	Default value	Description
bfh	*CSDLY*	8	00h	Reserved
c0h	*DM_LNL*	8	00h	insert the dummy line after active line(Dummy line low 8 bits) it's default value is 0x00;
c1h	*DM_LNH*	8	00h	insert the dummy line after active line(Dummy line high 8 bits)
c2h	*ESCH*	8	00h	Reserved
c3h	*EHUE*	8	00h	Reserved
c4h	*Dir_Ctrl*	8	40h	BIT[7] : Control the color of the line. 1'b1: change the color according to the cooresponding register. 1'b0: keep the color the same with the rows. BIT[6] : 1'b1: only show the straight lines. 1'b0: can show the curved lines when turning the wheel. BIT[3] : 1'b1: if BIT[6]=1'b0, show the curved lines, according to BIT[2:0]. 1'b0: only the straight lines. BIT[2:0]: the arc of the curved lines, if shown.
c5h	*B_STEP_LIMIT/ R_STEP_LIMIT*	8	aah	bit[7:4]:B_STEP_LIMIT ,control B gain step bit[3:0]:R_STEP_LIMIT ,contro lR gain step
c6h	*CB_CR_PURE*	8	aah	pure b or pure r threshold bit[7:4]:pure b threshold,multiplied by 4 bit[3:0]:pure r threshold,multiplied by 4
c7h	*OUT_STATE/ SENSIT_CNTL/ Cb_pure/ Cr_pure*	8	read only	read only bit [7]: 1: out state 0:not bit [2]: 1:High sensitivity 0:low sensitivity bit [1]: 1:Cb pure 0:not bit [0]: 1:Cr pure 0:not
c8h	*BLUE_GAIN_LOW _OUT*	6	0dh	bit[5:0]:The threshold of blue_gain_low_out
c9h	*BLUE_GAIN_HIG_ OUT*	6	30h	bit[5:0]:The threshold of blue_gain_high_out
cah	*LS_BASE_B_GAIN*	5	22h	bit[4:0]:base B gain for low sensitivity
cbh	*LS_BASE_R_GAIN*	5	15h	bit[4:0]:base R gain for low sensitivity
cch	*LS_GLGAINREG*	7	55h	Reserved
cdh	*Row_1_D*	8	40h	Reserved
ceh	*Row_2_D*	8	50h	Reserved
cfh	*Row_3_D*	8	60h	Reserved
d0h	*F_OFFSET*	8	00h	Reserved
d1h	*NF_OFFSET*	8	00h	Reserved
d2h	*IS_A_LIGHT & OUTDOOR_EN & GAIN_DIFF*	8	18h	Reserved
d3h	*RED_GAIN_LOW_ OUT*	6	09h	bit[5:0]:The threshold of red_gain_low_out
d4h	*RED_GAIN_HIG_O UT*	6	30h	bit[5:0]:The threshold of red_gain_low_out
d5h	*HBEGIN*	8	20h	Reseverd
d6h	*HEND*	8	50h	Reseverd
d7h	*VLINE*	8	00h	Reseverd
d8h	*VMODE*	4	00h	Reseverd
d9h	*VBEGIN1*	8	22h	Reseverd
dah	*VEND1*	8	32h	Reseverd
dbh	*VBEGIN2*	8	52h	Reseverd
dch	*VEND2*	8	62h	Reseverd
ddh	*REGISTER1*	8	90h	Reserved

Address	Name	Width	Default value	Description
deh	***HUE_COS***	8	7fh	Reserved
dfh	***HUE_SIN***	8	00h	Reserved
e0h	***H_HSYNC_EDGE***	8	00h	Reserved
e1h	***PRST2_F***	8	79h	Reserved
e2h	***DM_ROWL***	8	27h	Dummy line insert before active line low 8 bits
e3h	***DM_ROWH***	8	00h	Dummy line insert before active line high 8 bits
e4h	***PRST_R***	7	04h	Reserved
e5h	***PRST_F***	7	0dh	Reserved
e6h	***SHR_R***	7	0fh	Reserved
e7h	***SHR_F***	7	23h	Reserved
e8h	***TX_R***	7	28h	Reserved
e9h	***TX_F***	7	50h	Reserved
eah	***SHS_R***	7	55h	Reserved
ebh	***SHS_F***	7	69h	Reserved
ech	***READEN_R***	7	04h	Reserved
edh	***TX22_R***	8	75h	Reserved
eeh	***TX22_F2***	8	78h	Reserved
efh	***TX22_F***	8	89h	Reserved
f0h	***MODE_SEL***	1	1h	the high bit of TV_MODE; MODE_SEL=1,in pal or ntsc mode; MODE_SEL=0,in the normal mode;
f1h	***BYPASS0***	8	00h	Bit[0]:LensCorrection enable 0: enable, 1: disable Bit[1]:GammaCorrection enable 0: enable, 1: disable Bit[2]:Color Intrpolation enable 0: enable, 1: disable Bit[3]:Color Correction enable 0: enable, 1: disable Bit[4]: Color Space enable 0: enable, 1: disable Bit[5]:Saturation enable 0: enable, 1: disable Bit[6]:Contrast enable 0: enable, 1: disable Bit[7]:Datformat enable 0: enable, 1: disable
f3h	***Color_Sel_1***	8	11h	BIT[7:5]: Select color for the slope from the given 8 sets of color BIT[3:1]: Select color for the Bang! from the given 8 sets of color {BIT[4],BIT[0]}: 00: no numbers show beside the lines 01: only show numbers on the right side of the lines 10: only show on the left 11: show on both sides
f4h	***Color_Sel_2***	8	ebh	BIT[7:4]: Select color for the 1st row. BIT[3:0]: Select color for the 2nd row
f5h	***Color_Sel_3***	8	80h	BIT[7:4]: Select color for the 3rd row BIT[3:0]: Select color for the number.

Address	Name	Width	Default value	Description
f6h	***OverLay_Ctrl***	8	65h	BIT[7]: 1'b0: if outside switch is on, show the overlay, else, not show 1'b1: show the overlay. BIT[6:5]: Width select for the lines 00: 2 pixels wide 01: 4 pixels wide 10: 6 pixels wide 11: 8 pixels wide BIT[4]: the number mode 1'b1: the numbers are 1.5—1.0—0.5 1'b0: 2.0—1.5—1.0 BIT[3:2]: Select angle of the slope(V/H ratio) 00: 1, 01: 2, 10: 4, 11: 8 BIT[1]: 1'b1: solid rows 1'b0: dashed rows BIT[0]: 1'b1: solid slope 1'b0: dashed slope
f7h	***BANG_CTRL***	8	a5h	Bang
f8h	***Col_Width_Bottom***	8	86h	BIT[7:0]: shift the overlay up by given values.
Fah	***I2C_MODE_SEL***	1	01h	Bit[7:1]:resverd Bit[0] : 1'b1: I2C_FILTER module not bypass, 1'b0:I2C_FILTER module bypass
Fch	***PID_BME***	8	30h,RO	
Fdh	***VER_BME***	8	03h,RO	

8. Package Specifications

8.1 CLCC

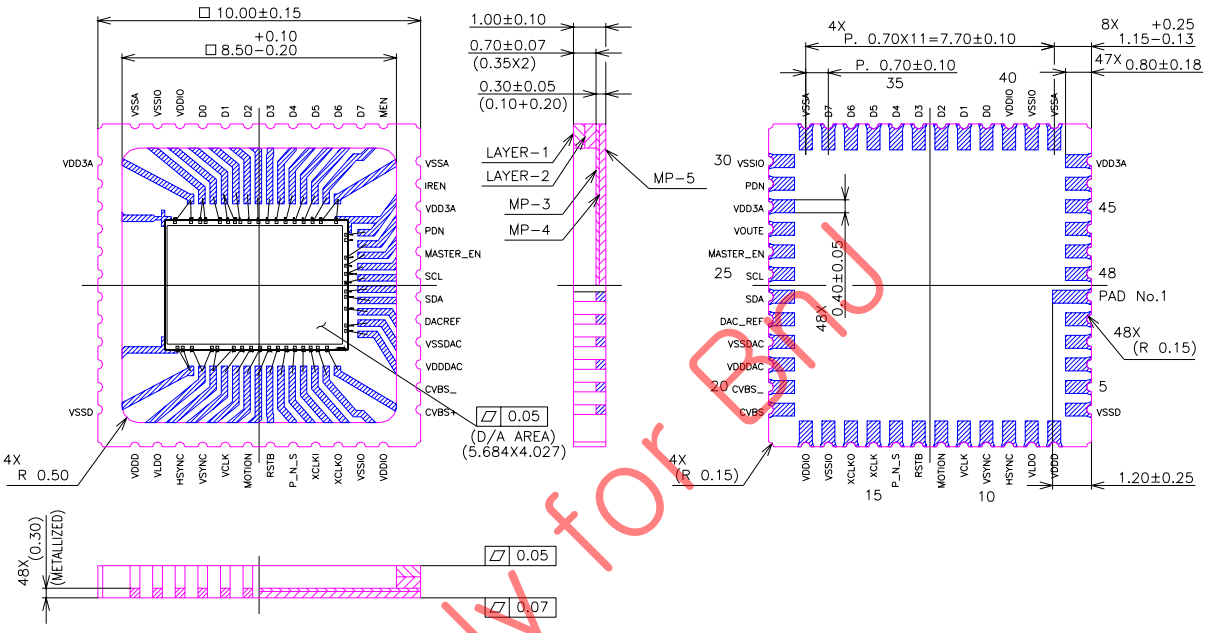

Figure 11. CLCC 48Pin Diagram

Table 7. The Pin Descriptions of the 48 Pin CLCC Package

Pin Number	Name	Pin Type	Function/Description
1	NC	–	No connect
2	NC	–	No connect
3	NC	–	No connect
4	NC	–	No connect
5	NC	–	No connect
6	VSSD	Ground	Digital ground
7	VDDD	Supply	Digital power: 1.5V
8	VLDO	Supply	Power supply for LDO: 1.8~3.3V(VLDO Voltage can't be higher than VDD3A)
9	HSYNC	Output	Horizontal reference output
10	VSYNC	Output	Vertical synchronization output
11	VCLK	Output	Video clock output
12	MOTION	Output	Motion detection. When the motion exists in the video, the output change to HIGH.

13	RSTB	Input	Hardware Reset, active low 0: Reset Mode 1: Normal Mode
14	P_N_S	Input	PAL/NTSC mode output selection: 1:PAL(Default) 0:NTSC
15	XCLKI	Input	System clock Input
16	XCLKO	Output	Oscillator clock Output
17	VSSIO	Supply	I/O ground
18	VDDIO	Ground	Power supply for I/O:1.7~ 3.3V
19	CVBS+	Output	Composite video active output,connect 75 ohm resistor to ground when single cablel transfer, connect 50 ohm resistor to ground when doubly cablel transfer.
20	CVBS-	Output	Composite video negative output, connect to round when single cablel transfer,connect 50 ohm resister to ground when doubly cablel transfer.
21	VddDAC	Supply	DAC power: 3.3V
22	VssDAC	Ground	DAC ground
23	DAC_REF	Input	External reference resistor for video DAC，680ohm resistor load for standard CVBS output.
24	SDA	I/O	SCCB serial interface data I/O
25	SCLK	I/O	Two-wire serial interface clock.
26	Mster_en	Input	I2C master enable: 0:Disable 1:Enable
27	PDN	Input	Power down mode ON/OFF selection: 0:OFF 1:ON
28	VDD3A	Supply	Analog power: 3.3V
29	IREN	Input	IR mode enable: 0:Disable 1:Enable
30	VSSA	Ground	I/O ground
31	MEN	Input	Mirror/Flip/Overlay Select
32~39	D7~D0	Output	Digital video output BIT[7]~BIT[0]: D[7:0] for 8-bit YUV, RGB, CCIR656 (D[7] MSB, D[0] LSB)
40	VDDIO	Ground	I/O ground
41	VSSIO	Supply	Power supply for I/O:1.7~ 3.3V
42	VSSA	Ground	Analog ground
43	VDD3A	Supply	Analog power: 3.3V
44	NC	–	No connect
45	NC	–	No connect
46	NC	–	No connect
47	NC	–	No connect
48	NC	–	No connect

RESTRICTIONS ON PRODUCT USE

- The information contained herein is subject to change without notice.
- BYD Microelectronics Co., Ltd. (short for BME) exerts the greatest possible effort to ensure high quality and reliability. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing BME products, to comply with the standards of safety in making a safe design for the entire system, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue. In developing your designs, please ensure that BME products are used within specified operating ranges as set forth in the most recent BME products specifications.
- The BME products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These BME products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of BME products listed in this document shall be made at the customer's own risk.